Design and Fabrication of a Microwave HEMT Oscillator Using a Phase-Locked Loop

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Abstract

The phase noise is one of the most critical figures for signal generators and the transceiver systems. Reducing phase noise still remains one of the most challenging aspects in oscillator design. This paper presents phase noise reduction technique of the HEMT oscillator using a phase-locked loop. Two HEMT oscillators for a C-band satellite receiver system are fabricated with different structures: one is made of voltage-controlled oscillator without a phase-locked loop and another uses a phase-locked loop frequency synthesizer, in order to demonstrate the phase noise reduction. The local oscillator operating at 2.45 GHz with output power higher than +5dBm, phase noise of -107 dBc@100Khz, a control voltage between 0 to 5 V and a single voltage supply of 5V.

Keywords: Phase noise, Voltage-controlled oscillator, Phase-locked loop, Satellite receiver, C-Band.

1. INTRODUCTION

All superheterodyne receivers use one or more local oscillators to convert an input frequency to an intermediate frequency before the signal is demodulated. In a real receiver, both the mixer used for converting the signal's frequency and the local oscillator will distort the signal and limit the receiver's ability to recover the modulation on a signal. The local oscillator creates random phase variations known as phase noise, which cannot be decreased except by improving the performance of the oscillator.

To address these needs in the microwave oscillators, there are several publications have deal with this phenomenon. For examples, paper [1] proposed the phase noise reducing using a dielectric resonator coupled by a high impedance inverter. In the paper [2], the proposed feedback and feedforward noise reduction techniques. In the [3] presents some basic characteristics of broadband negative resistance oscillator circuit.

In this study, a voltage-controlled oscillators using the phase-locked loop frequency synthesizer is presented. The local oscillator uses for C-band satellite receiver system. A schematic of the satellite receiver VINASAT can be found in Fig.1. The C-band (3.4 GHz–3.7 GHz) received signals first go through bandpass filter and then are next amplified by a LNA, after that go to the mixer. At the mixer, output produces consisting of the sum and difference frequencies and multiples of the wanted input signal and the local oscillator frequencies.

All that has come through the second bandpass filter and feeds them to the IF amplifier and into the cable. Typically, the output frequency = input frequency - local oscillator frequency. Hence, the local oscillator operate at 2.45 GHz to create the output frequency at 950 MHz to 1750 MHz.
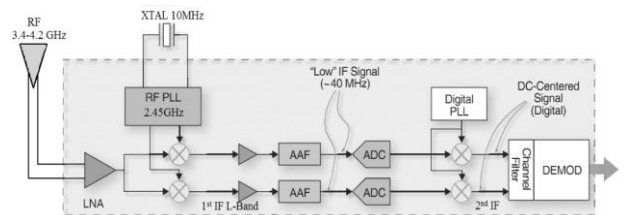

Figure 1: Signal chain for satellite receiver

Configuation of the oscillator was shown in Fig.2. The oscillator consists of the voltage-controlled oscillator (VCO) using HEMT transistor operate at 2.45 GHz, PLL frequency synthesizer using ADF-4113 and loop filter. Thefore, this paper include 3 main part: The first part is the design of voltage-coltrolled oscillator, the next part is the design phase-locked loop. Finally, the experimental results and analyses.
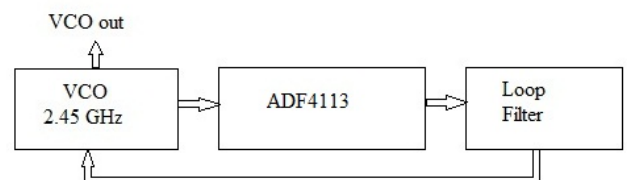

Figure 2: Configuation of phase-locked loop frequency synthesizer

2. DESIGN OF THE VOLTAGE- CONTROLLED OSCILLATOR

There are some architectures for designing VCOs. Based on the application and the specifications of the VCO, the Colpitts architecture was chosen, because of its simple design and fairly good characteristics. Moreover, the use of only one transistor in the topology was appealing in keeping the phase noise low. The Colpitts topology can be seen in Fig.3, with two possible configurations: one with the feedback from source to gate, and the other with feedback from drain to source. In order to create oscillator the feedback needs to be positive. Therefore either topology can be used.
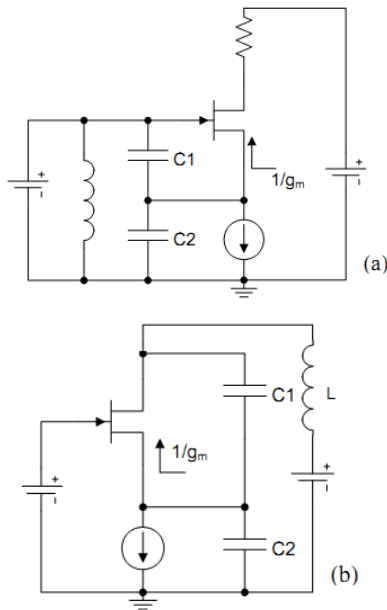
Figure 3: Basic Colpitts configutations

The voltage controlled oscillator (VCO) produces a fixed output frequency and must have extremely high stability as well as satisfying amplitude (in dBm). The design specifications of the VCO operates at 2.45 GHz to yield the intermediate frequency output ranging from 950MHz to 1750MHz. A single transistor capacitor feedback oscillator is shown in fig.4 [4].
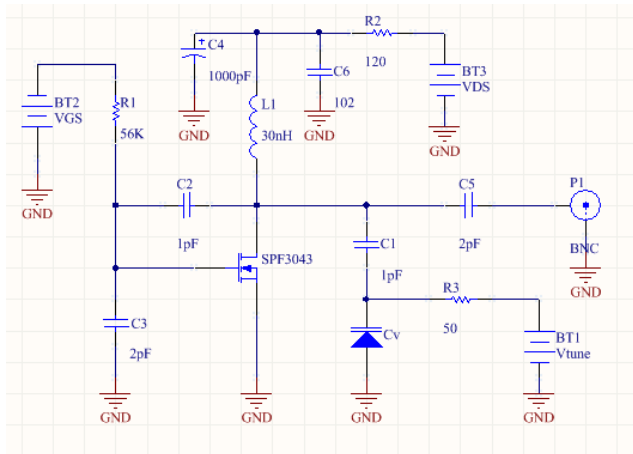

Figure 4: The schematic of C-band VCO

Because of frequency at C band, FET transistor is the number one solution to design C-band oscillator. Here, that makes it possible to select pHEMT GaAs SPF-3043. In order to maximize the output power while keeping low noise, the SPF-3043 was chosen to operate at Idss/2 and a Vds of 2.5V, Vgs of - 0.5V.

To achieve the center frequency of 2.45 GHz, The capacitors C_1 and C_2 were tuned and the value of the inductor was chosen around 3 - 4 nH. The next step, the SMV1232 varactor were chosen to place parallel to the $C_1 - C_2$ network.

In the fig.4, R_1 and R_2 are bias resistors; L_1, C_1, C_2, C_3, C_v play

an important role in the resonant circuit of Coltpitts schematic; C_5 is a coupling output capacitor; R_3 and C_v variable capacitors are utilized to tune the desired frequency.

3. DESIGN OF THE PHASE-LOCKED LOOP AND LOOP FILTER

A phase-locked loop is a feedback system combining a voltage-controlled oscillator and a phase comparator so connected that the oscillator frequency accurately tracks that of an applied frequency or phase-modulated signal. Phase-locked loops can be used, for example, to generate stable output frequency signals from a fixed low-frequency signal.

A simple block diagram of a voltage-based negative-feedback system is shown in Fig.5.
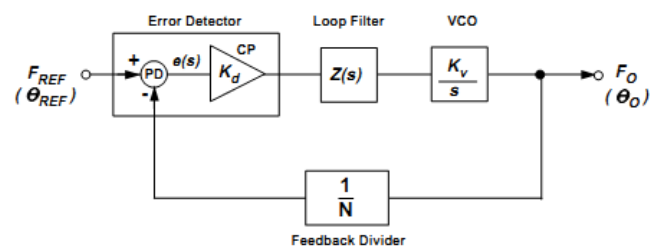

Figure 5: The schematic of phase-locked loop

The basic blocks of the PLL are the error detector, which composed a phase frequency detector and a charge pump, loop filter, VCO, and a feedback divider. Referring to Fig.5, a system for using a PLL to generate higher frequencies than the input, the VCO oscillates at an angular frequency of ω_0. A portion of this frequency/phase signal is fed back to the error detector, via a frequency divider with a ratio 1/N. This divided-down frequency is fed to one input of the error detector. The other input in this example is a fixed reference frequency/phase. The error detector compares the signals at both inputs. When the two signal inputs are equal in phase and frequency, the error will be zero and the loop is said to be in a "locked" condition. If we simply look at the error signal, the following equations may be developed.

$$e(s) = F_{REF} - F_0/N$$

When e(s) = 0, $F_0/N = F_{REF}$

Thus $F_0 = N\ F_{REF}$

In PLLs, the phase detector and charge pump together form the error detector block. When $F_0 \neq N\ F_{REF}$, the error detector will output source/sink current pulses to the low-pass loop filter. This smooths the current pulses into a voltage which in turn drives the VCO. The VCO frequency will then increase or decrease as necessary, by $K_v.\Delta V$, where K_V is the VCO sensitivity in MHz/Volt and ΔV is the change in VCO input voltage. This will continue until e(s) is zero and the loop is locked. The charge pump and VCO thus serves as an integrator, seeking to increase or decrease its output frequency to the value required so as to restore its input to zero.

In order to stable osillator frequency, we use the PLL frequency synthesizer ADF4113 from analog devices, the ADF4113 has been design to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters.

The ADF4113 consist of a low noise digital phase frequency detector (PFD), a prec ision charge pump, a programmable reference divider, programmable A and B counters, and a dual-modulus prescaler (P/P + 1). The A (6-bit) and B (13-bit) counters, in conjunction with the dual-modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R counter) allows selectable REF_{IN} frequencies at the PFD input.

Control of all the on-chip registers is via a simple 3-wire interface. The devices operate with a power supply ranging from 2.7 V to 5.5 V and can be powered down when not in use. The advantages of this part are low current consumption at low supply voltage and small dimensions.

The reference input signal is applied to the circuit at F_{REFIN} and is terminated in 50 Ω. This reference input frequency use 10MHz-TCXO FOX924E. In order to have a channel spacing of 200KHz, the reference input must be divided by 50, using the on-chip reference divider of the ADF4113.

The ADF4113 is an integer-N PLL frequency synthesizer, capable of operating up to an RF frequency of 4 GHz. In this integer-N type of synthesizer, N can be programmed from 96 to 262,000 in discrete integer steps. In this case, where an output frequency of 2450MHz is needed, and where the internal reference frequency is 200KHz, the desired N values will be 12250. The charge pump output of the ADF4113 (Pin 2) drives the loop filter. This filter Z(s) in Fig.6 is basically a 1st-order lag-lead type. In calculating the loop filter component values, a number of items need to be considered. In this paper, the loop filter was designed so that the overall phase margin for the system would be 45 degree and loop bandwidth about 12kHz.

All of these specifications are needed and used to come up with the loop filter components values shown in Figure 6.
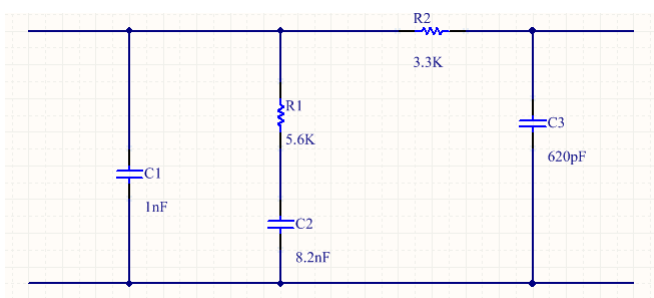

Figure 6: Schematic of loop filter

The loop filter output drives the VCO, which is fed back to the RF input of the PLL synthesizer and also drives the RF Output terminal. A Π-circuit configuration is used to provide 50-ohm matching between the VCO output, the RF output and the RF_{IN} terminal of the ADF4113.

In a PLL system, it is important to know when the system is in lock. In Figure 8, this is accomplished by using the MUXOUT signal from the ADF4113. The MUXOUT pin can be pro-grammed to monitor various internal signals in the synthesizer.

One of these is the LD or lock-detect signal. When MUXOUT is chosen to select lock detect, it can be used in the system to trigger the output power amplifier. The completed circuit was shown in fig.7.
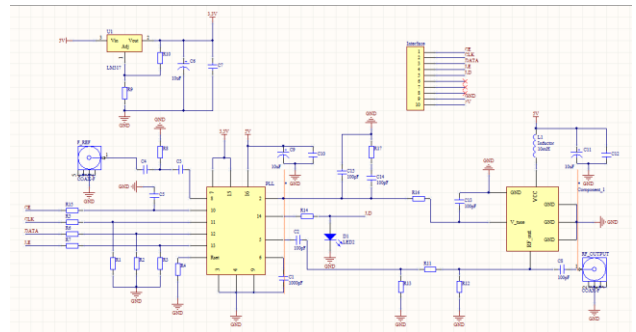

Figure 7: Schematic of the oscillator

4. RESULTS AND ANALYSES

After the schematic circuit has been modified, the print circuit board of the VCO using PLL was created and shown in fig. 8.
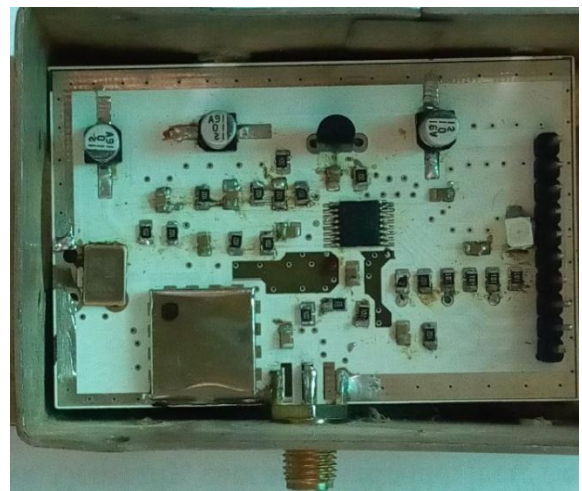

Figure 8: Layout of the VCO using ADF4113

The manufactured circuits are tuned to oscillator around 2.45 GHz by slightly adjusting a voltaged-varicap tuning. The phase noise is measured by a spectrum analyzer (NS-265 from 9 KHz to 26.5 GHz) with condition of a 50 Khz resolution bandwith. The oscillator without PLL show the phase noise characteristics of –97dBc/Hz at 100Khz offset frequency, otherwise the oscillator using PLLs show the phase noise characteristics of –107.8dBc/Hz. Figure 9, 10 shows the measured power spectrums of the manufactured oscilltors. The comparition of the manufactured oscilltors is summarized in Table 1.
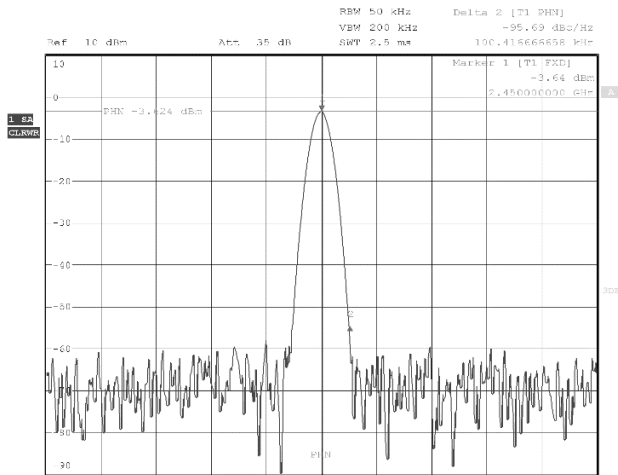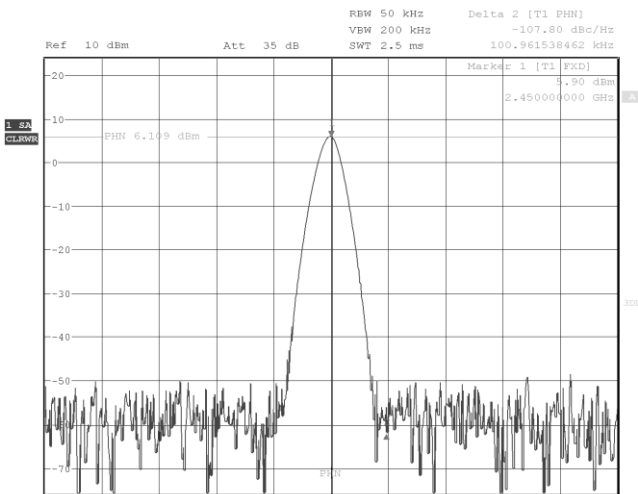
Figure 9: The phase noise of VCO without PLL

Figure 10: The phase noise of VCO using phase-locked loop

Table 1: Comparison measurement results

Parameters	VCO	VCO with PLL
Oscillation Frequency	2.45GHz	2.45GHz
Output Power	-3.64 dBm	5.9 dBm
Phase Noise @100 KHz	-95.96 dBc/Hz	-107.80 dBc/Hz

5. CONCLUSION

In this paper, the phase noise reduction of microwave HEMT oscillators using a phase locked loop has been successfully designed and fabricated. The performance of the VCO using PLL shows a phase noise reduction by 12dB. Applying this method to MESFET or HBT oscillators would show a better phase noise performance. The circuit has a compact size of 4cm×6cm, which is welcome in many applications. At the time of writing this paper, the VCO was used for the LNB working at C-band.

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