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Investigation of D Flip flop designing Using INDEP with Bi-Triggering (Trig01) NAND Gate Approach

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Abstract

In today's scenario, the world is changing by degrees. The rapid changes in the technology teach us to revolutionize with this. Nowadays all the gadgets are small. They are fast and prices are cheap compared to the old era. The component density and size are increases with time. Researchers are continuously experimenting with Scaling of transistors. By the advancement of new technologies, the circuit size compactness and pros and cons of the devices can be easily realized. When the chip density of the circuit increases, the power consumption of the circuit is also increases. This limits the reliability and cost of the circuit. It also suffers with design stoutness, yielding, signal reliability, and procedure variability. The researchers have to compromise between all of them. As the power consumption is the most important parameter for VLSI designing. For the designing of any circuit, the performance and power consumption are directly relay on the selection of the logic gates. By the scaling of these basic gates all the parameters can be modified. In this paper, a new approach (INDEP with Trig 01) is used to design D flip flop. The simulation tool used for designing of D flip flop is Mentor Graphics with Pyxis Schematic 10.5 Version. The technology is 130nm with 1V supply voltage. The planned circuit is amalgamation of INDEP with Trig01 Approach. Simulation is done to calculate the values of throughput delay, power expenditure, and product of power throughput.

Keywords - INDEP, Trig 01, Power delay and D flip flop.

I. INTRODUCTION

IC designing is a prominent task nowadays since technology is growing advance day by day. Since scaling of transistor means number of transistor in a circuit increases, increases the packing density of the circuit. Perhaps containing a high power density and reduces the supply voltage to the circuits. Therefore, mostly in all integrated circuits, the number of sequential and combinational devices increases [5]. To overcome the demand of the compact devices the researchers have to compromise between the power dissipation and reliability.

Nowadays the technology is moving towards the faster speed and low cost computing system. This can be facilitate by the increases the number of transistor as well as the chip density. To scale the transistor rapidly, causes many errors like toughness, mild errors and variability in the process [2, 10]. The logic gates are the vital building blocks for each digital design. Therefore, by saving the individual power to the logic gates, the overall efficiency will increased. In the proposed D flip flop, two methods is used. The power dissipation may be lower down by reducing the supply voltage. Seeing as the fact that there is a quadratic relation among them but throughput delay may increase. Therefore, a mid way has to be finding to design any circuit. The introduction of the paper should explain the nature of the problem, previous work, purpose, and the contribution of the paper. The contents of each section may be provided to understand easily about the paper.

II. LITERATURE REVIEW

The leakage power in deep submicron technology plays an important role for designing any digital circuit. Power of circuit classified as dynamic power and static power. Static power is the energy devoted without the transition of CMOS transistor [7]. The dynamic power is the power consumed, during the transition of the transistor. The dynamic power is very dominant for the latest technologies. There are many factors that affect the circuit's power like drain induce barricade lowering, tunneling phenomenon, punch through effect and low inversion current [3, 14] that are shown in Fig 1. The most important reason for increasing the leakage power is amplify the leakage sub-threshold power.

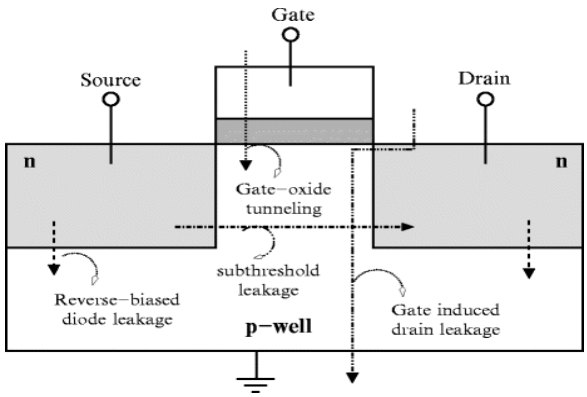


Figure 1: Tunneling phenomenon of CMOS Transistor

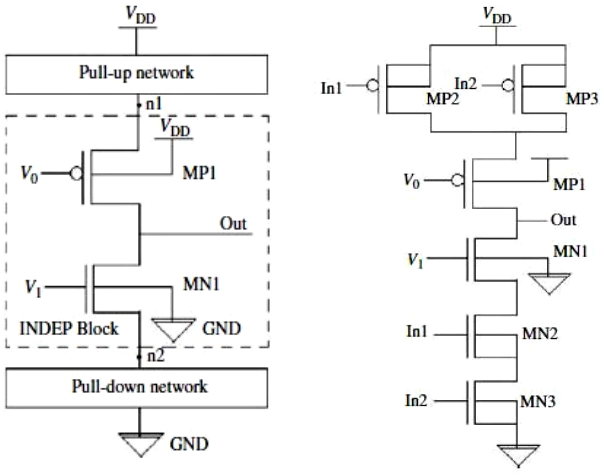
This is due to the current flowing between drain and source of the transistor within weak inversion area. Due to scaling of the transistor, the power supply is low so the threshold voltage is

also downward. As reference, voltage decreases the sub, threshold leakage power increases and vice versa. The gate oxide layer works as passivating layer between channel and gate [9]. To enhance the channel capacity, the thickness of this layer kept thin. Nevertheless, as oxide layer kept thinner the oxide barrier voltage alters. When positive gate voltage is applied, some positive charges stuck in the oxide layer and cause current flow (known as tunneling current).

Mutual charge in depletion area is poise by the electrode charges of three regions i.e. gate, source and drain regions. When voltage across the drain increases, the p-n junction depletion layer increases and extend to the gate. Therefore, the drain have larger load for complementary charge, parting small load to the gate [11]. Consequently, the charge nearby the gate region retains charge via attract additional carriers to the channel. Outcome of that the device threshold voltage lowered.

III. INDEP APPROACH

Input Dependant (INDEP) technique is low leakage power and transistor level design. This can be a midway between power and throughput delay. By stacking the transistors, it will decrease the leakage current but suffers with large delay. By using the proper selection of input terminal to the transistors, this problem overcomes. In this approach, two additional transistors (call INDEP transistors) applied between pull - down and pull-up transistors [12] to diminish the leakage power. All the transistors have same threshold voltage. For each input combinations INDEP transistors are associated with pull down and pull up network. The drain points (Fig 2a) of INDEP transistors (MN_1 and MP_1), are jointly connected to form output. The two points (n_1 and n_2) are connected to pull down and pull up transistors. MP1 linked to n_1 and out port so it passes the high logic level (by complete voltage swing). MN1 associated to output and n2 node to pass the low voltage level.



(a) **(b)**

Figure 2 (a) The INDEP approach.
(b) NAND with INDEP approach

Table 1: working of INDEP Transistor

In1	In2	V_0	V_1
0	0	Any input signal	Any input signal
0	1	Turn on the MP1/MN1	turn-on the MP1/MN1
1	0	Turn on the MP1/MN1	turn-on the MP1/MN1
1	1	Any input signal	Any input signal

In (Fig 2b), as both inputs In1 and In2 are equal and then other inputs V_0 and V_1 are connected to any input signal either high or low. For different stages of (V_0 and V_1) the input signal connected to turn on the MN_1 and MP_1, transistors [8].

IV. TRIG 01 APPROACH

In this technique, nMOS and pMOS are use as bi triggering switch, positioned next to the voltage divider circuit [4, 6]. By the help of the voltage divider circuit, the operating voltage separated in two parts. Both the transistors connected by two separate inputs nods as shown in the Fig. 3.

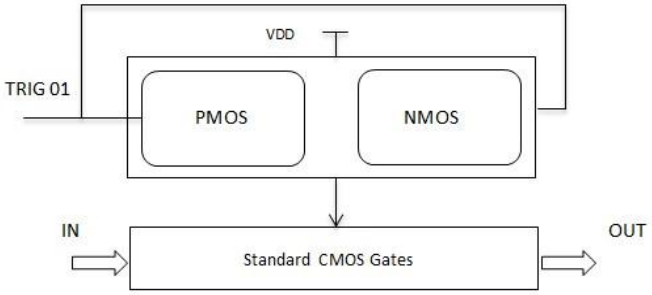


Figure 3: The Trig 01 approach

Thus, the input and output terminal is straightforwardly coupled to CMOS circuit. When PMOS and NMOS transistors are on, half power mode triggered. By applying, the '0' and '1' trigger pulses to PMOS; it is switch on and off. Likewise, by applying the control signals as '1' and '0' NMOS transistor is switch on /off [13]. To operate the circuit in full mode, both NMOS and PMOS worked in a closed loop. Thus, the CMOS circuit gives full mode power. The main advantage is this circuit is that it will not affect the circuit performance.

V. MATHEMATICAL TREATMENT OF BASIC NAND GATE

NAND gate is the main element of the designing of D-flip flop. The main parameters of any circuit are power consumption and propagation delay. The average power of any gate is the product of drain current and supply voltage. A usual CMOS NAND gate considered by using the pull-up connection contains two pMOS transistors connected in parallel. In addition, the pull-down connection contains two nMOS transistors, connected in series [15]. As the size of the

transistor decreases, increase the leakage power. The simulated diagram and waveform of basic NAND gate is shown by Fig 4.

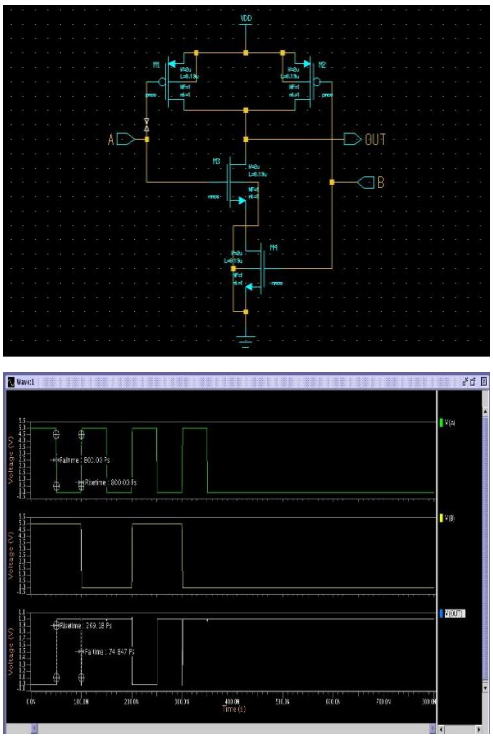


Figure 4: Basic NAND gate and input and output waveforms

In the proposed approach, input dependent with trigger 01 method used to design the NAND gate. The simulated diagram and the output waveforms of the proposed approach are shown in the Fig. 5. The common parameters used for the designing of both the gates are shown in the table 1.

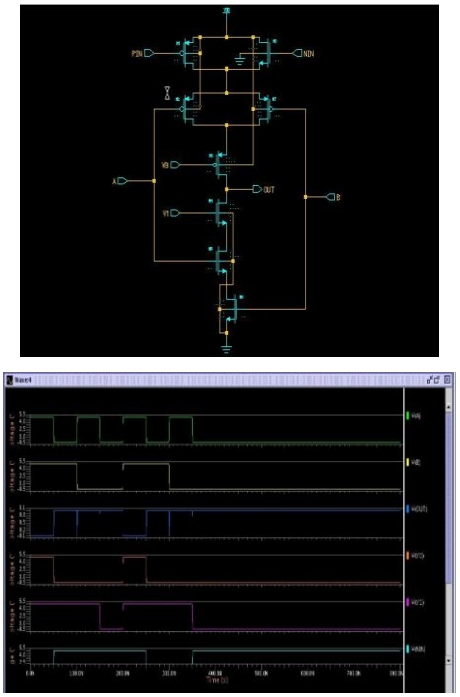


Figure 5: Proposed NAND gate

The proposed gate simulation is performed Mentor Graphics Back End Tool with Pyxis Schematic 10.5 version at 130nm CMOS technology.

Table 2: Common Parameters for NAND Gate

Parameter	Mathematical values
ε_{ox} (oxide permittivity)	3.5 x 10^{-13} F/cm
t_{ox} (oxide thickness)	$2.8 * 10^{-9}$
$V_{DS} = V_{Gs}$	1V
c_{ox}	$1.2548 * 10^{-4}$
V_{DD}	1.8V
No. of transistor	8

The transmission delay (τ) is the time taken by the input signal to reach at the output terminal. It is also call as logic holdup during propagation of the signal. This is calculating by the average of high to low transition and low to high transition of output pulse.

Table 3: Designing parameters of nMOS and pMOS transistor

Parameter	**Mathematical values**
For NMOS	
V_{Ton} (Threshold voltage) = 0.3732V	V_{Gs}=V_{DS}= 1V
W=2u and L=0.13u	I_D=$1.5109 * 10^{-5}$A
K'= $7.745 * 10^{-6}$	μ_n = $6.1728 * 10^{-2}$
For PMOS	
V_{Top} (Threshold voltage) = -0.3095V	V_{Gs}=V_{DS}=1V
W=2u and L=0.13u	I_D=$2.21616 * 10^{-5}$A
K'= $1.7806 * 10^{-9}$	μ_p = $1.4191 * 10^{-5}$

VI. D FLIP FLOP USING THE PROPOSED NAND GATE

Flip-flops are single bit storage; bi-stable multivibrator circuits used in all digital devices. It is a delay circuit, used to modify the state of input signal until the next clock cycle is arrived. It has single input (Data) terminal and complimentary output terminals.

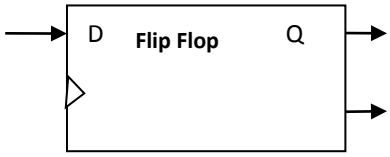


Figure 6: D Flip-flop

When the input to the D terminal is high, the output of the flip-flop would be high and when the low pulse arrived at the D terminal, the output is low [7, 10]. Therefore, the flip – flop

is now in reset mode. A square signal used, as a clock wave that frequently repeats on some frequency.

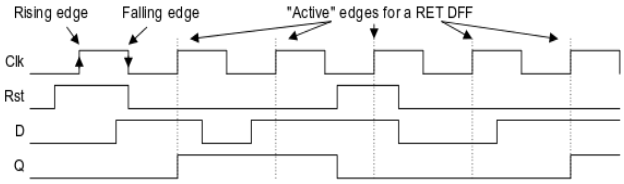


Figure 7: Rising edge triggering behavior of D flip flop

Nonetheless, it would be quite meaningless, as the output of the D flip-flop be always changing on each input pulse apply to the data input. Therefore, another clock signal applied to the input to separate input data to the rest of flip-flop's circuitry. However, this would be rather pointless since the output of the flip-flop would constantly change with every clock pulse. The timing waveforms shown in Fig. 7 demonstrate rising edge triggering behavior. D flipflop can come into a meta-stable condition, when the data input and control input altered exactly the same time. This condition does not resolve immediately and provide oscillatory output. If the D input is stable instantly before and after the clock edging, the flip-flop provides stable state.

Table 4: Truth Table for the D-type Flip Flop

Clock	D	Q	Q'	Circuit description
0	X	Q	Q'	No change in memory
1	0	0	1	Reset
1	1	1	0	Set

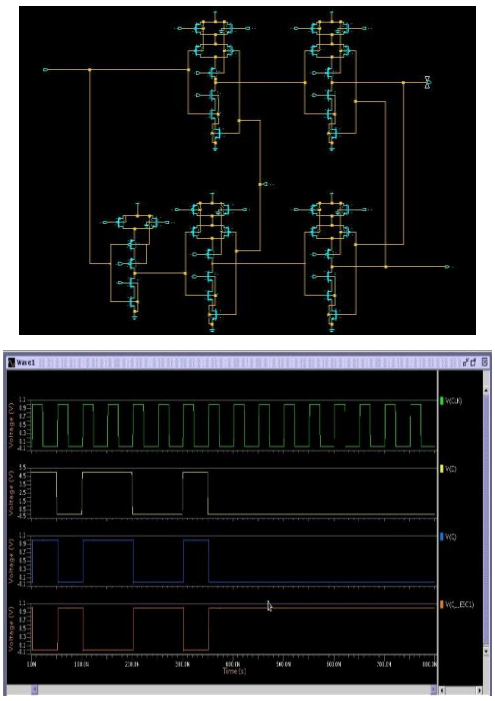


Figure 8: input and output waveforms of positive edge D flip flop

When no clock pulse is applied then circuit has no change in memory whatever the input D is. After applying the clock pulses the flip-flop start working and follow the data input. According to data, input circuit must be set or reset.

VII. RESULTS AND DISCUSSION

The proposed parameters like power dissipation and propagation holdup obtained by the output waveform (figure 8). The obtained values of simulated results and mathematical results are almost same.

Parameters	Values
Node voltage A	5.0v
Node Voltage B	5.0v
Output Delay	938.5273psec
Vdd	1V
Power dissipation	1.8336p watts
Temperature	27°C

The processed parameters verified by computer simulation at Mentor Graphics Back End Tool with Pyxis Schematic 10.5 Version. The supply voltage for simulation is 1V at room temperature. The simulation is performed by ELDO Simulator with 130nm CMOS technology as well as waveform is obtained by EZ Wave Schematic.

VIII. CONCLUSION

The both base and lector with trig 01 approach, used to simulate NAND Gate design. Modeling and simulation has performed for NAND and D flip-flop circuit. The various parameters and results obtained, shown in table 2. The projected NAND gate reduces the power dissipation via addition of two supplementary transistors. One is INDEP transistor among the pull up and pull down network other one is in above the pull up network.

Simulated outcome specify the proposed design challenges in feat such as power, holdup and power delay results. By the analytical analysis, the proposed approach is much better in throughput and leakage power. In future, the modified circuit promote for other flip flop also. This approach, possibly use for other combinational and sequential circuits.

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REFERENCES

[1] Anurag, G. Singh, V. Sulochana, Low Power Dual Edge Triggered Static D Flip-Flop, *International Journal of VLSI design & Communication Systems (VLSICS), 4(3)*, 2013, 23-29.

[2] A. K. Dadoria, K. Khare and R. P. Singh, Sleepy Lector: A Novel Approach for Leakage Reduction in DSM Technology, *IEEE 6th International Conference on Cloud System and Big Data Engineering (Confluence)*, 664-669, 2016.

[3] M. Shakya and S. Agrawal, Design Low Power CMOS D-Flip Flop using Modified SVL Techniques, *International Journal of Research and Analytical Reviews (IJRAR), 5*, 2018, 55-65.

[4] N. A. Sabu and K. Batri, Review of Low Power Design Techniques for Flip-Flops, *International Journal of Pure and Applied Mathematics, 120 (6)*, 2018, 1729-1749.

[5] K. Shilpa and G. D. Kumar, Clock Related Flip-Flop with Sleepy Transistor Merging For Power Saving", *International Journal of Advanced Research in Computer and Communication Engineering, 5 (3)*, 2016, 946-950.

[6] R. V. Tambat and S. A. Lakhotiya, Design of Flip-Flops for High Performance VLSI Applications using Deep Submicron CMOS Technology, *International Journal of Current Engineering and Technology, 4(2)*, 2014, 769-774.

[7] K. Sharma *et al.*, Designing a Novel Power Efficient D-Flip-Flop using Forced Stack Technique, *International Journal of Computer Applications, 68 (9)*, 2013,25-30.

[8] A. Lakshmi and P.C. Reddy, Design and Implementation of Conventional D Flip-Flop for Registers, *International Journal of Computer Applications, 181(39)*, 2019, 24-28.

[9] P. K. Chakravarti and R.Mehra, Layout design of D Flip Flop for Power and Area Reduction, *International Journal of Scientific Research Engineering & Technology (IJSRET*), 2015.

[10] K. Srilatha *et al.*, Implementation of D Flip-Flop using CMOS Technology, *International Journal of Trend in Scientific Research and Development (IJTSRD), 4(3)*, 2020.

[11] P. Gupta and R. Mehra, Low power design of SR flip-flop using 45nm technology, *IOSR Journal of VLSI and Signal Processing, 6(2)*, 2016, 54-57.

[12] G. V. Rao *et al.*, Designing of SR and D Flip Flop using Reversible Logic, *International Journal of Advanced Science and Technology, 29 (5)*, 2020, 10429- 10436.

[13] N. Verma and D. Mishra, New approach to design D-fip fop and two bit down counter using optical micro-ring resonator for high speed data processing, *SN Applied Sciences, 542*, 2020.

[14] S. Dharani and M. A. Asuvanti, D Flip Flop Using AVLG Technique with Static Body Biasing Using Cadence Virtuoso Tool, *Journal of Electronic Design Engineering, 5(3)*,2019, 16-21.

[15] S.Sheik *et al.*, Design of New Dual Edge Triggered Sense Amplifier Flip-Flop with Low Area and Power Efficient, *International Journal of Applied Engineering Research, 13 (9)*, 2018, 6780-6789.