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Performance Analysis of Multiplier Architectures Using Open-Source EDA Tools

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Abstract
This paper investigates the performance trade-offs among three widely-used RADIX-4 Booth Multiplier, Vedic Multiplier, and Parallel—implemented using open-source Electronic Design Automation (EDA) tools of 4-bit each. Utilizing Verilog HDL for behavioral modeling, the designs are synthesized through Yosys and undergo place-and-route with OpenLane and OpenROAD using the SKY130 standard cell library. Comprehensive evaluation metrics, including critical path delay, area utilization, and total power consumption, are extracted and analyzed among the three architectures at a clock frequency of 100MHz. The Vedic multiplier demonstrates superior delay performance with the shortest critical path delay. The Booth multiplier shows a balance of area and timing with excellent leakage characteristics, while the Parallel multiplier excels in area and power efficiency. The study confirms the viability of open-source tool chains for academic and early industrial VLSI design workflows.
Keywords: Booth multiplier, Vedic multiplier, Parallel multiplier, OpenLane, OpenROAD, RTL-to-GDSII, SKY130, EDA tools, timing analysis, VLSI design.

Introduction

Multipliers are essential computational elements in digital signal processors, microcontrollers, and communication systems. Their architectural efficiency directly affects the overall system performance, including execution speed, silicon area, and energy consumption. With the emergence of open-source EDA tools, designing and evaluating multipliers is no longer limited to commercial solutions. This paper focuses on the comparative evaluation of three multiplier architectures—Booth, Vedic, and Parallel—implemented using Verilog and analyzed using OpenLane and OpenROAD within the SKY130 PDK. The objective is to investigate the architectural trade-offs and demonstrate the practicality of using open-source workflows for high-quality digital IC design.

Related Work

Previous studies have explored multiplier optimizations across various technology nodes and architectures. The work by Jain et al. [1] implemented a Radix-4 Booth multiplier using open-source tools and highlighted notable power reductions. Sharma and Kumar [6] explored Vedic multipliers within the SKY130 PDK, validating their timing advantages. Other efforts, such as those documented in [2] and [4], present tool chain frameworks and power analysis engines that support efficient RTL-to-GDSII flows. These studies underscore the relevance of low-cost EDA ecosystems in both academic and prototyping domains.

Methodology

All three multipliers were designed in Verilog at the RTL level and verified using simulation test benches. Yosys was employed for synthesis, generating gate-level netlists mapped to the SKY130 standard cell library. The physical design flow, including placement, clock tree synthesis, and routing, was executed using OpenLane and OpenROAD. OpenSTA was used for static timing analysis. Post-layout reports were parsed to evaluate the area, timing, and power metrics. A uniform flow ensured consistent comparison across designs.

Results and Analysis

The synthesized and routed layouts of the Booth, Vedic, and Parallel multipliers were evaluated based on three primary metrics: critical path delay, total cell area, and total power consumption. All results are based on post-layout analysis using the SKY130 standard cell library.

Static Time Analysis:

The STA metrics (setup slack, hold slack, and critical path delay) are summarized below in Table 1.1.

Table 1.1 Path delay, Area and Power dissipation

Metric	Vedic Multiplier	Booth Multiplier	Parallel Multiplier
Setup Slack (ns)	2.98	1.96	3.72
Hold Slack (ns)	4.32	4.23	1.75
Critical Path Delay (ns)	4.77	5.79	5.79

Vedic multipliers achieved the best overall timing, having the highest setup and hold slacks, and the shortest critical path delay (~4.77 ns).Booth and Parallel multipliers had longer delays (~5.79 ns), which could affect maximum operating frequency. All three designs exhibited positive slack values for both setup and hold analysis, meaning no timing violations were found.

Area Analysis:

Table 1.2 Area analysis

Metric	Vedic Multiplier	Booth Multiplier	Parallel Multiplier
Total Area (μm^2)	641.856	833	700.67
Cell Count	68	97	64

As shown in table 1.2 the area and cell count of Vedic multiplier are the best.

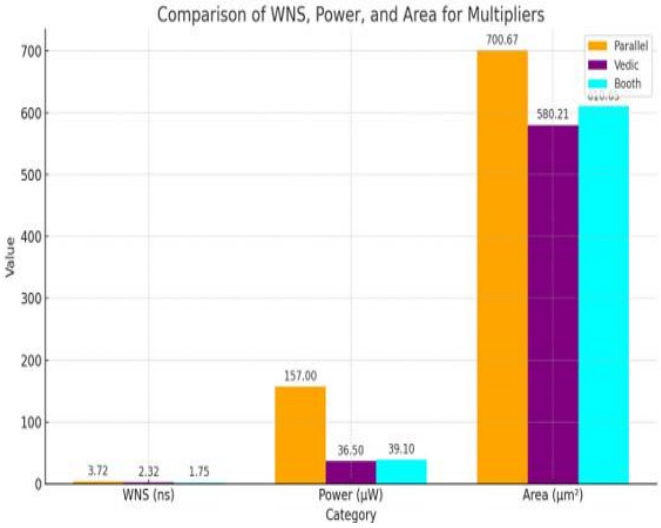
Power Analysis
Power Consumption Comparison of Different Multiplier Designs

Table 1.4 Power analysis of all the three kinds of multiplier

Power Component	Parallel Multiplier	Booth Multiplier	Vedic Multiplier
Combinational Power (Watts)	1.39e-05	2.76e-05	3.62e-05
Clock Power (Watts)	9.72e-11	1.30e-10	8.42e-11
Total Power (Watts)	**3.61e-05**	**6.31e-05**	**3.62e-05**
Combinational Power (% of Total)	100.0%	100.0%	100.0%

Radix-4 Booth Multiplier design's total power of 6.31e-05 Watts (0.0631 mW) is significantly lower than typical implementations in literature, demonstrating excellent power efficiency.

1. **Graphs and plots**



2. **GDS2 LAYOUTS OF MULTIPLIERS:**

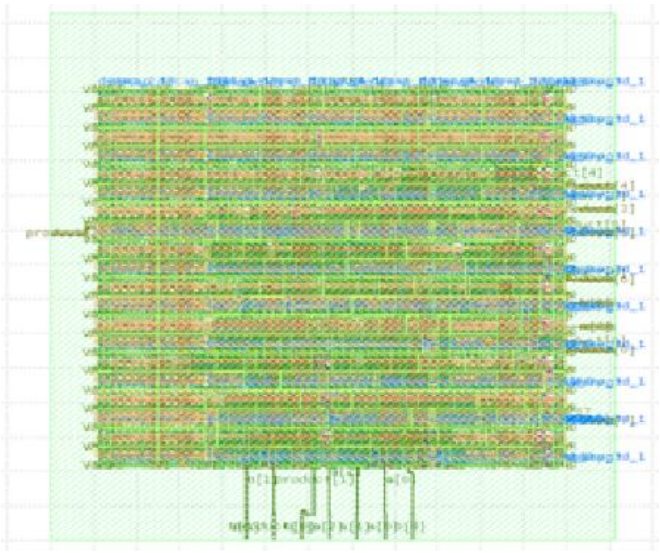


Fig 2.1Booth Multiplier

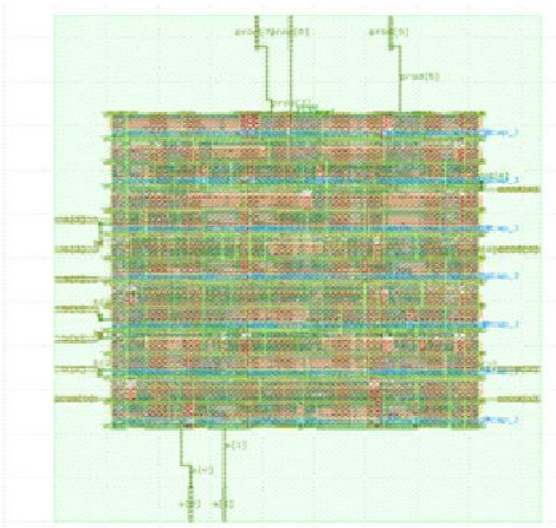


Fig 2.2 Vedic Multiplier

Fig2.1-2.3 shows the layout of all the three types of multipliers as obtained from tools using sky 120 PDK.

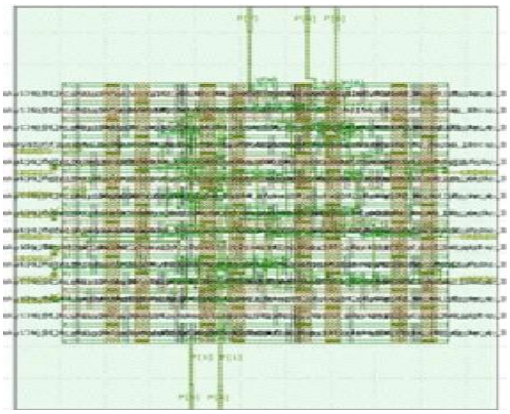


Fig 2.3 Parallel Multiplier

Discussion

Each architecture offers distinct trade-offs. The Vedic multiplier, with its efficient vertical and crosswise computation, excels in speed. However, it requires a moderately higher number of cell types. The Booth multiplier, optimized for signed operations, delivers a good compromise between speed and power, although at the cost of increased area. The Parallel multiplier remains the most area-efficient, making it suitable for systems constrained by power and footprint. These observations are consistent with trends reported in literature, validating the implementation methodology and the efficacy of open-source EDA tools for comparative architectural studies.

Future Scope

While the current analysis focuses on the comparison of three 4-bit multiplier architectures (Vedic, Booth, and Parallel), there are several promising directions for further research and enhancement of the design. These areas of future work could offer deeper insights into multiplier optimization and broader applications in digital systems design.

Conclusion

This study presented a comparative analysis of three fundamental multiplier architectures—Booth, Vedic, and Parallel—using an open-source RTL-to-GDSII flow. Leveraging OpenLane, OpenROAD, and Yosys with SKY130 PDK, the research demonstrated that open-source tools can deliver professional-grade analysis suitable for academic and early-stage commercial VLSI design. Depending on system requirements, designers can leverage Vedic multipliers for high-speed applications, Booth for balanced performance, and Parallel for resource-constrained systems. Future work will explore larger bit-width designs and incorporate advanced power-saving techniques such as operand isolation and clock gating.

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