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Power Gated Match Line Sensing Content Addressable Memory

Belma Joseph and Dr.S.Jayanthy

ME VLSI Design student (IEEE Member),
(HoD, Embedded system Technologies)
Sri Ramakrishna Engineering College, Coimbatore

Abstract

A Content-Addressable Memory (CAM) compares input search data against stored data, and returns the address of the matching data. CAM offers high-speed search function in a single clock cycle [6]. In the conventional Content-Addressable Memory (CAM), equal power is consumed to determine if a stored word is matched to a search word or mismatched. A match line (ML) sensing scheme is used for match decision. Due to its parallel match-line (ML) comparison, CAM consumes more power. So, robust, high-speed and low-power sense amplifiers are highly sought-after in CAM designs. This paper introduces a new CAM with an effective gated-power technique to reduce average power consumption and comparatively reduces the sensing delay [1]. Feedback loops is employed to auto-turn off the power supply to the comparison elements and hence reduce the average power consumption. During the evolution stage ML is not fully charged to VDD. So sensing delay is also comparatively reduced. This paper compares the power dissipation and sensing delay of proposed CAM with existing structures. The performance comparisons and analysis made in Mentor Graphics EDA Tool using tsmc 180 nm.

Index Terms: Content-addressable memory (CAM), match line sensing, SRAM.

INTRODUCTION

A Content-Addressable Memory (CAM) compares input search data, and returns the address of the matching data. It has a single clock cycle throughput making them faster than other hardware and software search systems. CAMs can be used in various applications requiring high search speeds [6]. In Internet, a message such an as e-mail

or a web page is transferred by breaking up the message into small data packets of a few hundred bytes, and, each data packet individually through the network. Then these packets are routed through the intermediate nodes of the network (called router). These packets are reassembled at the destination to reproduce the original message. The main function of a router is to compare the destination address of a packet with all possible routes, in order to choose the best match one. A CAM is a good choice for implementing this lookup operation due to its fast search capability.

In general, a CAM has three operation modes: READ, WRITE, and COMPARE, among which "COMPARE" is the main operation as CAM rarely reads or writes. Fig. 1 shows a block diagram of a CAM core with an incorporated search data register and an output encoder. [6] By loading an n bit word in to the search data register, compare operation will start. Then the search data are broadcast into the memory banks through n pairs of complementary search-lines (SL) and directly compared with every bit of the stored words using comparison circuits. Each stored word has a ML that is shared between its bits to convey the comparison result. An encoder will identify the location of matched word, as shown in Fig. 1(a). The MLs are held at ground voltage level while both SL and ~SL are at VDD during pre-charging phase. During evaluation stage, complementary search data is broadcast to the SL and ~SL. When mismatch occurs in any CAM cell (for example consider the first cell of the row D="1";~D= "0"; SL= "1"; ~SL="0"), transistor P3 and P4 will be turned on, charging up the ML to a higher voltage level. To detect the voltage change on the ML a sense amplifier (MLSA) is used and amplifies it to a full CMOS voltage output. If no charge up path unchanged. In this work, a power-gated ML sense amplifier is proposed to improve the performance of the CAM ML comparison in terms of power and robustness. Also reduces the peak turn-on current at the beginning of each search cycle of operation.

The remaining part of paper is organized as follows. In Section II, introduces the gated power technique. In section III performance analyses are presented. In section IV concludes this paper.

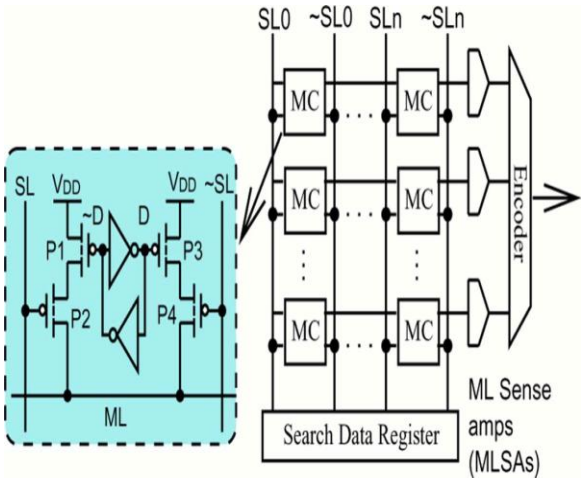


Fig.1. Block diagram of a conventional CAM.

II. GATED- POWERML SENSE AMPLIFIER DESIGN

The proposed CAM architecture is depicted in Fig.2 [1].The CAM cells are organized into rows (word) and columns (bit). Each cell has the same number of transistors as the conventional P-type NOR CAM (shown in Fig. 1) and use a similar ML structure. The "COMPARISON" unit, i.e., transistors M1-M4, and the "SRAM" unit, i.e., the cross-coupled inverters, is powered by two separate metal rails, namely VDDML and the VDD, respectively. The VDDML is independently controlled by a power transistor (Px) a feedback loop that can auto turn-off the ML current to save power. The use of having two separate power rails of (VDD and VDDML) is to completely isolate the SRAM cell from any possibility of power disturbances during COMPARE cycle.

As shown in Fig. 2, the gated-power transistor Px, is controlled by a feedback loop, denote as "Power Control" which will automatically turn off Px once the voltage on the ML reaches a certain threshold. At the beginning of each cycle, the match line is initialized by a global control signal EN.At this time, signal EN is set to low and the power transistor Px is turned OFF. Thus this will make the signal ML and C1 initialized to ground and VDD, respectively. Then, the signal EN turns HIGH and initiates the COMPARE phase.

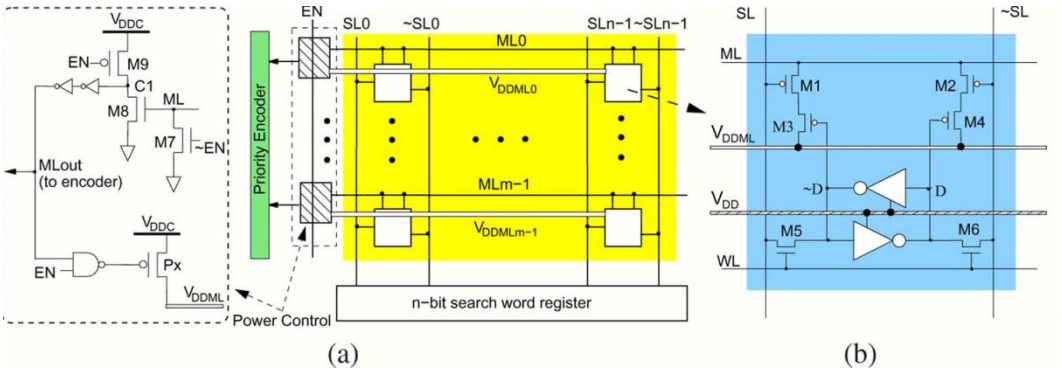


Fig. 2. (a) Proposed Content Addressable Memory (CAM) architecture. (b) Each CAM cell is connected to two power rails, for the compare transistors, for the SRAM transistors. The rail of a row is connected to the power network through a pMOS device, which is used to limit the transient current.

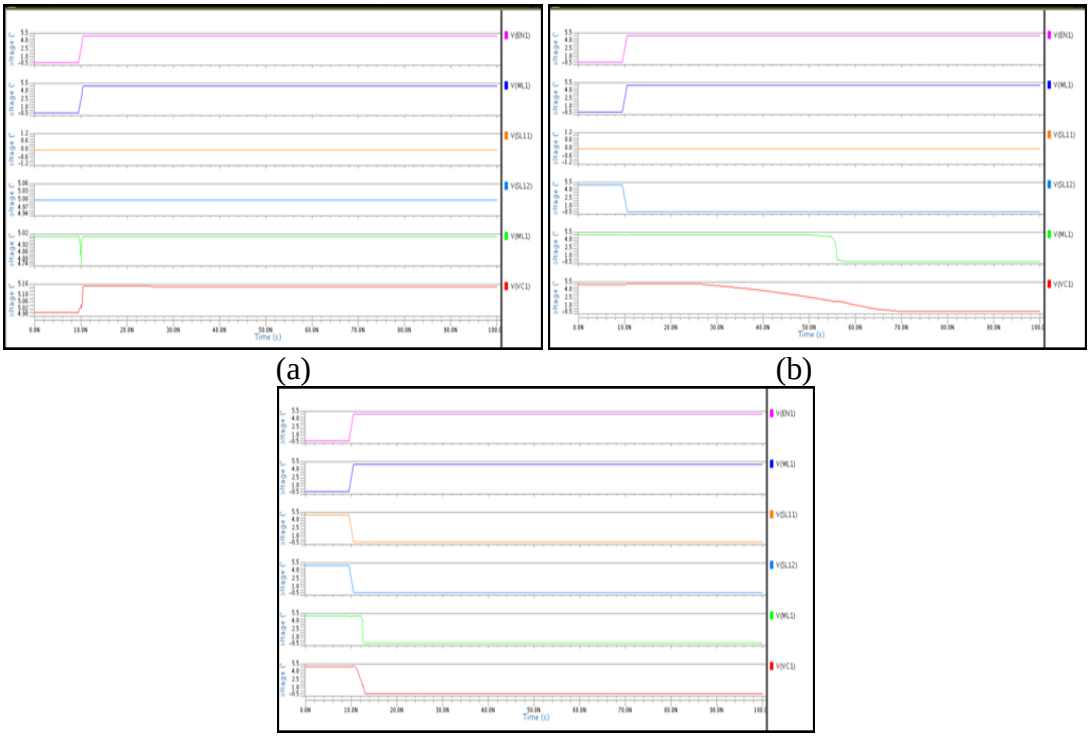
If one or more mismatches happen, the ML will be charged up. All the cells of a row will share the limited current offered by the transistor Px, despite whatever number of mismatches. When the voltage of the ML reaches the threshold voltage of transistor M8 (i.e., Vth8), voltage at node C1 will be pulled down. After a very minor delay, the NAND2 gate will be toggled and so the power transistor Px is turned off again. As a result, the ML is not fully charged to VDD, but limited to voltage slightly above the threshold voltage of M8.

Fig. 3 shows the simulation results of the proposed power controller of CAM structure for 3 cases (matched case, mismatched case, and partial matched case).During matched case ML case has high output and VC1 charged to high voltage

and during mismatched case ML and VC1 discharged to a low voltage. One can see that, the slopes of the ML, node C1 and node ML out depend on the number of mismatches. When more mismatches happen, the ML and node C1 change faster.

Less number of mismatches will slow down the transition of node C1 and results in a longer delay to turn off transistor Px.

With the introduction of the power transistor Px, the driving strength of the 1-mismatch case is about weaker than that of the conventional design. Thus it offers both low-power and high-speed operation.



(a) (b)

(c)

Fig. 3. Waveforms of some important nodes during evaluation of the proposed design.(a) Output wave form for matched case.(b) Output wave form for partial matched case.(c) Output wave form for mis- matched case

III.PERFORMANCE COMPARISONS

In this section, performance of the proposed design is evaluated and compared with the conventional circuit and those in [2], [7] as references. In [2], the power consumption is limited by the amount of charge injected to the ML at the beginning of the search. In [7], a similar concept is utilized with a positive feedback loop to boost the sensing speed. Both designs are very power efficient. The proposed design consumes slightly lower power when compared with [2],[4] and [7] .The proposed design has comparatively low sensing delay hence increases the searching speed of CAM which is more favorable for VLSI design.

Power Consumption

Fig. 4 illustrates the average power consumption of the proposed design and compared the performances with other three existing designs. The power-gated transistor is turned off after the output is obtained at the sense amplifier. So the proposed technique has lower average power consumption. Also because of reduced voltage swing on design. Because the EN signal turns off transistor Px of each row and column hence the SL buses do not need to be pre-charged, which in turn saves power on the SL buses.

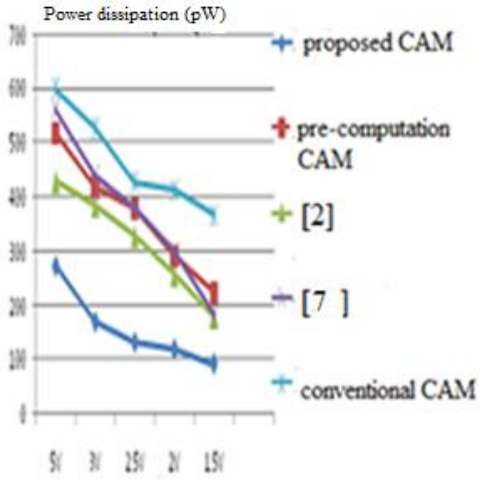


Fig .4. Total average power consumption of the four designs.

Sensing Delay

The sensing delay comparison is shown in Fig. 5 where the proposed design improves the performance when compared with the conventional design. This figure also shows that sensing delay increases dramatically when supply voltage enters the near-sub threshold region.

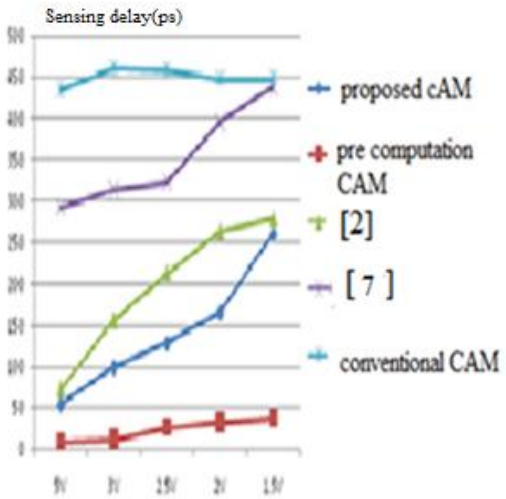


Fig. 5 sensing delay of the four designs

Sensing delay is defined as the sensing delay of the 1-mismatch.

IV. CONCLUSION

An effective method for high speed and low power CAM is proposed in this paper. A power gated ML sensing technique offers several advantages like average power consumption, boosted search speed when compare with conventional design.

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