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Space Vector Based Novel and Simple Unified Pulsewidth Algorithm for Induction Motor Drives

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Abstract

This paper presents a space vector based simple and novel unified pulsewidth modulation (UPWM) algorithm for induction motor drives by using the concept of offset time. The conventional space vector PWM (SVPWM) algorithm divides the zero state time equally between two zero states. But, the variation of zero voltage vector time duration results in generation of various discontinuous PWM (DPWM) algorithms. The conventional SVPWM algorithm requires the calculation of sector and angle information, which increases the complexity of the algorithm. Hence, to reduce the complexity, the proposed PWM algorithm uses the concept of offset time and does not use sector and angle information. In the proposed algorithm, first, a general expression for offset time in terms of zero voltage vector time partition parameter (μ) and modulation angle (δ) is derived. Then by varying μ and δ various DPWM algorithms have developed. To validate the proposed algorithm, several numerical simulation studies have been carried out on v/f controlled induction motor drive at different modulation indices and results are presented and compared.

Introduction

Due to the inventions of fast switching power semiconductor devices and motor control algorithms, a growing interest is found in a more precise pulsewidth modulation (PWM) method. During the past decades several PWM algorithms have been studied extensively. Various PWM methods have been developed to achieve wide linear modulation range, less switching loss, less total harmonic distortion (THD) and easy implementation and less computation time. A large variety of algorithms for PWM exist, and a survey of these was given in [1]. There are two popular approaches for the implementation of PWM algorithms, namely triangular comparison (TC) approach and space vector (SV) approach. For a long period, TC approach based PWM methods were widely used in most applications. The earliest modulation signals for TC approach based PWM are sinusoidal. But, the addition of the zero sequence signals to the sinusoidal signals results in several non-sinusoidal signals. Compared with sinusoidal PWM (SPWM) algorithm, nonsinusoidal PWM algorithms can extend the linear modulation range for line-to-line voltages. Different zero-sequence signals lead to different nonsinusoidal PWM modulators [2]-[3].

Nowadays, due to the development of digital signal processors, SVPWM has become one of the most popular PWM methods for three-phase inverters [4]. It uses the SV approach to compute the duty cycle of the switches. The main features of this PWM algorithm are easy digital implementation and wide linear modulation range for output line-to-line voltages. The equivalence between TC and SV approaches has studied in [5] and concluded that SV approach offers more degrees of freedom compared to TC approach. The conventional SVPWM algorithm distributes the zero voltage vector time duration equally among the two zero states. However, the unequal distribution of zero voltage vector times results in various DPWM algorithms, which is illustrated in [2]-[3], [6]. To generalize all DPWM algorithms along with SVPWM algorithm, a generalized DPWM algorithm has developed in [7]-[8]. As the SPWM and SVPWM algorithms have continuous modulating signals, the switching losses are more. Nowadays, the discontinuous PWM (DPWM) algorithms are becoming popular. In the DPWM algorithms, the modulating signals are clamped to either positive dc bus or negative bus for a total period of 120 degrees in every fundamental cycle. Hence, the switching losses can be reduced up to one third compared with continuous PWM algorithms. Also, the DPWM algorithms will give superior performance over SVPWM algorithm at higher modulation indices [3].

However, the conventional SV approach requires the calculation of angle and sector information and hence the complexity of the algorithm increases. To reduce the complexity of the PWM algorithm a novel modulation algorithm is developed by using the concept of offset time [9]-[11]. However, these algorithms require different offset times for the generation of different PWM algorithms. Moreover, to reduce the complexity involved in conventional approach, a novel approach is developed in [12] by using the concept of imaginary switching times.

In this paper, a space vector based novel and simple UPWM algorithm for induction motor drives is presented. This paper is based on the concept of offset time. Instead of using different offset times for different PWM algorithms, a generalized offset time is derived in this paper in terms of zero voltage vector time partition

parameter (μ) and modulation angle (δ) from which various DPWM algorithms have developed. Moreover, this paper reveals the relationship between the reference phase signals and imaginary switching times, the relationship between offset time and different PWM algorithms. Furthermore, the simulation of the proposed

PWM method is discussed and simulation results are provided to validate the drawn conclusions.

Conventional SVPWM Algorithm

The main purpose of the voltage source inverter (VSI) is to generate a three-phase voltage with controllable amplitude, and frequency. A general 2-level, 3-phase VSI feeding a three-phase induction motor is shown in Fig 1.

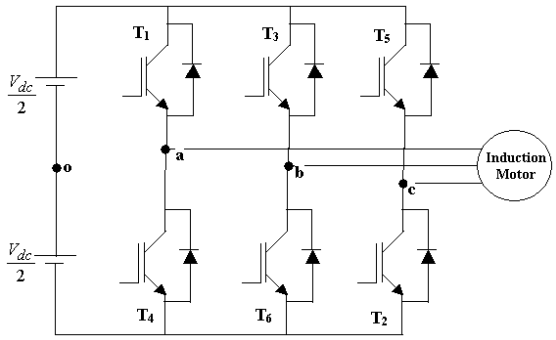

Figure 1 : Two-level, three-phase voltage source inverter fed induction motor

From Fig. 1, it can be observed that the two switching devices on the same leg cannot be turned on and cannot be turned off at the same time, which will result in the uncertain voltage to the connected phase. Thus the nature of the two switches on the same leg is complementary. The switching-on and switching-off sequences of a switching device are represented by an existence function, which has a value of unity when it is turned on and becomes zero when it is turned off. The existence function of a VSI comprising of switching devices T_i is represented by S_i, i = 1, 2, . . . , 6. Hence, S_1, S_4 which take values of zero or unity respectively, are the existence functions of the top device (T_1) and bottom device (T_4) of the inverter leg which is connected to phase 'a'.

$$S_1 + S_4 = 1;\ S_3 + S_6 = 1;\ S_5 + S_2 = 1 \tag{1}$$

As seen from Fig 1, there are totally six switching devices and only three of them are independent. The combination of these three switching states gives out eight possible voltage vectors. At any time, the inverter has to operate one of these voltage vectors. Out of eight voltage vectors, two are zero voltage vectors (V_0 and V_7) and remaining six (V_1 to V_6) are active voltage vectors. In the space vector plane, all the voltage vectors can be represented as shown in Fig 2.

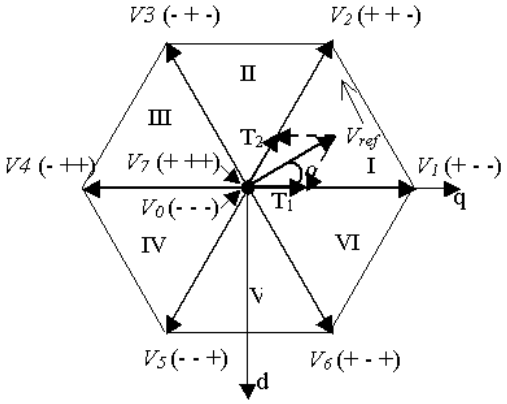

Figure 2 : Voltage space vectors produced by a voltage source inverter

For a given set of inverter phase voltages (V_{an}, V_{bn}, V_{cn}), the space vector can be constructed as

$$V_s = \frac{2}{3}\left(V_{an} + V_{bn} e^{j\frac{2\pi}{3}} + V_{cn} e^{j\frac{4\pi}{3}} \right) \tag{2}$$

From (2), it is easily shown that the active voltage vectors or active states can be represented as

$$V_k = \frac{2}{3} V_{dc} e^{j(k-1)\frac{\pi}{3}} \qquad \text{where k} = 1,2,...,6 \tag{3}$$

By maintaining the volt-second balance, a combination of switching states can be utilized to generate a given sample in an average sense during a subcycle. The voltage vector V_{ref} in Fig.2 represents the reference voltage space vector or sample, corresponding to the desired value of the fundamental components for the output phase voltages. But, there is no direct way to generate the sample and hence the sample can be reproduced in the average sense. The reference vector is sampled at equal intervals of time, T_s referred to as sampling time period. Different voltage vectors that can be produced by the inverter are applied over different durations with in a sampling time period such that the average vector produced over the subcycle is equal to the sampled value of the reference vector, both in terms of magnitude and angle. As all the six sectors are symmetrical, here the discussion is limited to sector-I only. Let T_1 and T_2 be the durations for which the active states 1 and 2 are to be applied respectively in a given sampling time period T_s. Let T_z be the total duration for which the zero states are to be applied. From the principle of volt-time balance T_1, T_2 and T_z can be calculated as:

$$T_1 = \frac{2\sqrt{3}}{\pi} M\left[Sin(60^o - \alpha)\right] T_s \tag{4}$$

$$T_2 = \frac{2\sqrt{3}}{\pi} M\left[Sin(\alpha)\right] T_s \tag{5}$$

$$T_Z = T_s - T_1 - T_2 \tag{6}$$

In the SVPWM strategy, the total zero voltage vector time is equally distributed between V_0 and V_7. Further, in this method, the zero voltage vector time is distributed symmetrically at the start and end of the subcycle in a symmetrical manner. Moreover, to minimize the switching frequency of the inverter, it is desirable that switching should take place in one phase of the inverter only for a transition from one state to another. Thus, SVPWM uses 0127-7210 in first sector, 0327-7230 in second sector and so on.

Proposed UPWM Algorithm

Instead of equal distribution of zero state time among the zero voltage vectors, the proposed algorithm uses unequal distribution of zero state time. By varying the zero voltage vector time variation as $T_0 = \mu T_z$ and $T_7 = (1-\mu) T_z$, various discontinuous PWM (DPWM) algorithms can be developed. Since all of these different schemes are based on the division of zero voltage vector time, it is possible to derive the general expression that is used to generate all the possibilities. Thus, to generate the various DPWM methods along with the SVPWM algorithm, the proposed algorithm has developed. Moreover, to reduce the complexity involved in conventional SVPWM algorithm, the proposed PWM algorithm uses reference phase voltages.

The time durations of the active voltage vectors can be represented in terms of phase voltages or line to line voltages as given in (7) – (8) [9]-[12].

$$T_1 = \frac{T_s}{V_{dc}} V_{an} - \frac{T_s}{V_{dc}} V_{bn} \equiv \frac{T_s}{V_{dc}} \left(V_{an} - V_{bn}\right) \equiv T_s \frac{V_{ab}}{V_{dc}} \tag{7}$$

$$T_2 = \frac{T_s}{V_{dc}} V_{bn} - \frac{T_s}{V_{dc}} V_{cn} \equiv \frac{T_s}{V_{dc}} \left(V_{bn} - V_{cn}\right) \equiv T_s \frac{V_{bc}}{V_{dc}} \tag{8}$$

The switching times in each sector in terms of line voltages and maximum and minimum voltages in each sector are given in Table 1. Also, in a balanced three-phase system as shown in Fig 1, the sum of the three phase voltages is zero. Then the voltage between neutral of the induction motor and reference point of the DC source, which is also known as common mode voltage or neutral voltage, is determined from (9).

$$V_{no} = \frac{V_{dc}}{3}\left(S_1 + S_3 + S_5 - \frac{3}{2}\right) \tag{9}$$

Table 1 : Device switching times expressed in terms of reference line-line voltages

	Sector-I	**Sector-II**	**Sector-III**	**Sector-IV**	**Sector-V**	**Sector-VI**
$V_{\max}$	V_{an}	V_{bn}	V_{bn}	V_{cn}	V_{cn}	V_{an}
$V_{\min}$	V_{cn}	V_{cn}	V_{an}	V_{an}	V_{bn}	V_{bn}
T_1	$T_s\frac{V_{ab}}{V_{dc}}$	$T_s\frac{V_{ba}}{V_{dc}}$	$T_s\frac{V_{bc}}{V_{dc}}$	$T_s\frac{V_{cb}}{V_{dc}}$	$T_s\frac{V_{ca}}{V_{dc}}$	$T_s\frac{V_{ac}}{V_{dc}}$
T_2	$T_s\frac{V_{bc}}{V_{dc}}$	$T_s\frac{V_{ac}}{V_{dc}}$	$T_s\frac{V_{ca}}{V_{dc}}$	$T_s\frac{V_{ba}}{V_{dc}}$	$T_s\frac{V_{ab}}{V_{dc}}$	$T_s\frac{V_{cb}}{V_{dc}}$

where $V_{\max}$ and $V_{\min}$ represents maximum and minimum phase voltages in every sampling interval.

The general expression for the average neutral voltage, V_{no}, can be determined using the method of space vector modulation and the voltages of the three-phase voltage source converter. For example, in first sector $V_{\max} = V_a$, $V_{\min} = V_c$. For a balanced three-phase supply system, $V_b = -(V_{\max} + V_{\min})$. Hence, the switching times can be rewritten as (10).

$$T_1 = \frac{2V_{\max} + V_{\min}}{V_{dc}}T_s;\ T_2 = \frac{-V_{\max} - 2V_{\min}}{V_{dc}}T_s;\ T_z = \left(1 - \frac{V_{\max} - V_{\min}}{V_{dc}}\right)T_s \tag{10}$$

The average neutral voltage is

$$V_{no} = \frac{1}{T_s}\left(V_{no1}T_1 + V_{no2}T_2 + V_{no0}T_0 + V_{no7}T_7\right) = \frac{V_{dc}}{6}\left(\frac{T_2 - T_1}{T_s}\right) + \frac{V_{dc}}{2}(1-2\mu)\left(\frac{T_z}{T_s}\right) \tag{11}$$

By substituting (10) in (11), the expression for neutral voltage can be obtained as

$$V_{no} = \frac{V_{dc}}{2}(1-2\mu) + (\mu - 1)V_{\max} - \mu V_{\min} \tag{12}$$

Hence, the modulating voltage waveforms can be represented as given (13).

$$V_{in}^{*} = V_{in} + V_{no} \qquad i = a,b,c \tag{13}$$

The actual gating times can be calculated by using the concept of imaginary switching times. The value of imaginary switching time is directly related to the phase

voltage and can be expresses as given in (14).

$$T_{an} = \frac{V_{an}}{V_{dc}} T_s; \quad T_{bn} = \frac{V_{bn}}{V_{dc}} T_s; \quad T_{cn} = \frac{V_{cn}}{V_{dc}} T_s \tag{14}$$

These switching times could be negative when the phase voltage is negative and hence these are called as imaginary switching times. The maximum and minimum imaginary switching times can be evaluated in each sampling interval from (15).

$$T_{\max} = \max(T_{an}, T_{bn}, T_{cn}); \quad T_{\min} = \min(T_{an}, T_{bn}, T_{cn}) \tag{15}$$

Then the general relation between the actual gating times and the modulating voltage waveforms is as given in (16).

$$T_{gi} = \frac{T_s}{2}\left(1 + \frac{2V_{in}^*}{V_{dc}}\right) \tag{16}$$

By substituting (12) and (13) in (16), the general expression for actual gating times can be obtained as

$$T_{gi} = T_{in} + T_{offset} \tag{17}$$

where $T_{offset} = T_s(1-\mu) + (\mu - 1)T_{\max} - \mu T_{\min}$ (18)

In the implementation of the proposed offset time based unified PWM algorithm, the zero voltage vector time partition parameter (μ) can take any form (constant or time-varying) ranging between 0 and 1. The choice of μ affects the average neutral voltage. In the conventional SVPWM algorithm, as the zero voltage vector time is distributed equally, μ is generally taken as 0.5. If μ is either 0 or 1, each switching device ceases to switch for a total of 120 degrees per fundamental cycle. Hence, the switching losses and effective inverter switching frequency are significantly reduced. As the modulating signals are discontinuous, these PWM algorithms are also known as DPWM algorithms or bus-clamping PWM algorithms. The selection of μ gives rise to an infinite number of possible PWM algorithms, some of which have been referred in [7]-[8]. To obtain the various DPWM algorithms, μ is taken as given (19).

$$\mu = \text{sgn}\left[\cos(3\omega t + \delta)\right] \tag{19}$$

where sgn(X) is 1, 0 and –1 when X is positive, zero, and negative, respectively. By varying the modulation angle δ, various DPWM algorithms are generated. The SVPWM, DPWMMIN and DPWMMAX algorithms can be obtained for μ = 0.5, 1 and 0 respectively. Moreover, DPWM0, DPWM1, DPWM2 and DPWM3 can be obtained for δ = π/6, 0, - π/6 and - π/3 respectively. Finally, the expression for the modulating waveform of unified PWM algorithm can be given as

$$V_{in}^{*} = \frac{V_{dc}}{2}\left(\frac{2 * T_{gi}}{T_s} - 1\right) \tag{20}$$

Simulation Results and Discussions

To validate the proposed UPWM algorithm, several numerical simulation studies have been carried on v/f controlled induction motor drive. For the simulation studies, the average switching frequency of the inverter is taken as 3 kHz and the dc link voltage is taken as 600 V. The modulating wave form at different modulation indices are given in Fig. 3 – Fig. 5 along with the reference phase voltage. Also, the modulating wave, pulse pattern, steady state stator current wave, phase voltage and line voltages for different modulation indices are given in Fig.6–Fig.21. Moreover, the harmonic distortions of steady state current along with the total harmonic distortion (THD) values are given in Fig. 22-Fig. 37. From the simulation results it can be observed that the continuous PWM (CPWM) algorithms (SPWM and SVPWM) give superior performance at lower modulation indices and DPWM algorithm give superior performance at higher modulation indices. Moreover, with the CPWM and DPWM algorithms, the dominant harmonic components are found at f_{sw} (3 kHz) and $1.5 f_{sw}$ (4.5 kHz) respectively.

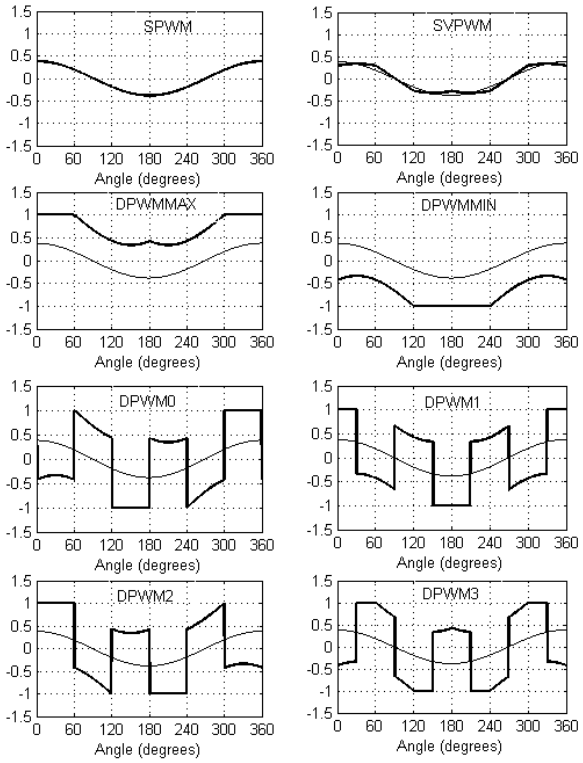

Figure 3 : Modulation waveforms of various PWM methods at M=0.3

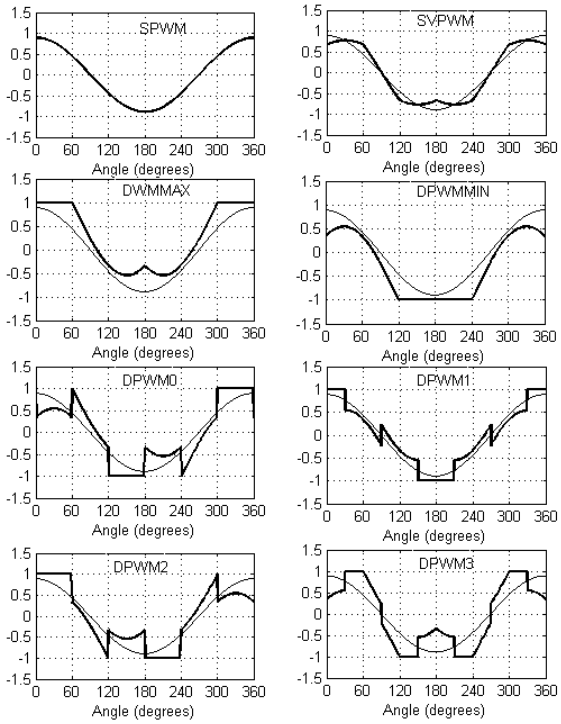

Figure 4 : Modulation waveforms of various PWM methods at M=0.7

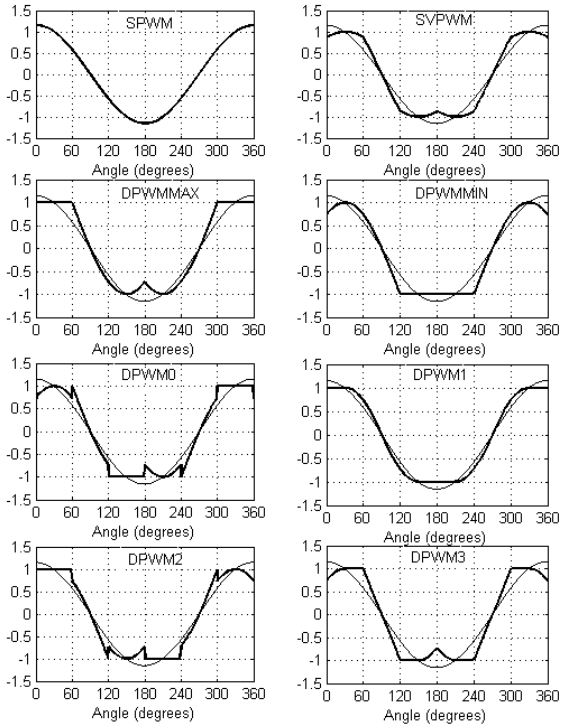

Figure 5 : Modulation waveforms of various PWM methods at M=0.906

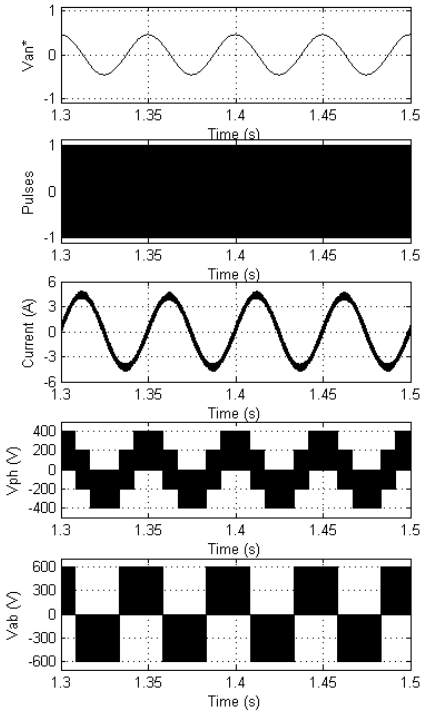

Figure 6 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for SPWM algorithm at f=20 Hz and M=0.36

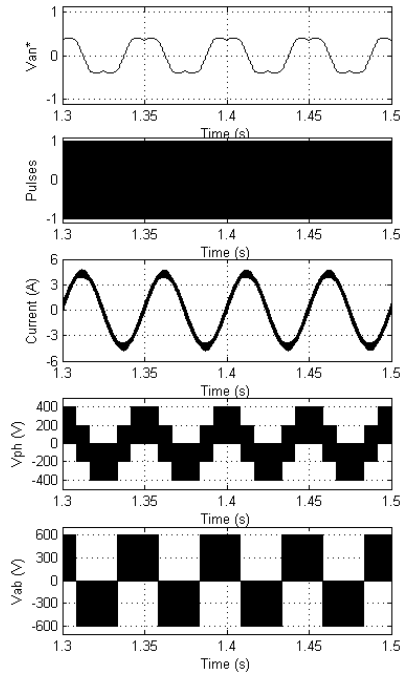

Figure 7 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for SVPWM algorithm at f=20 Hz and M=0.36

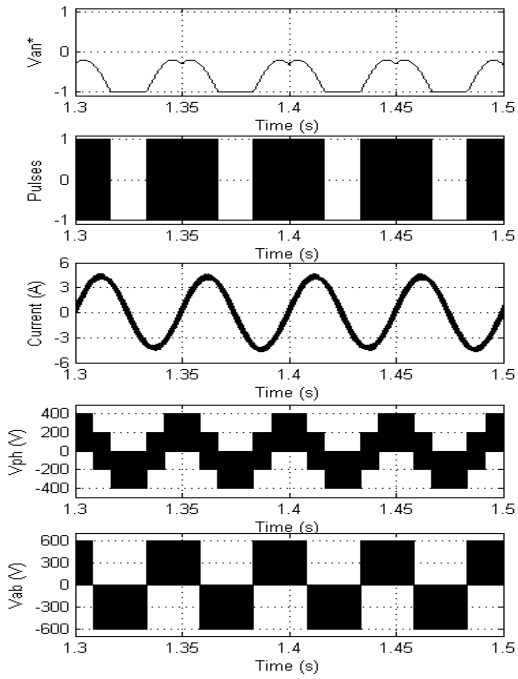

Figure 8 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for DPWMMIN algorithm at f=20 Hz and M=0.36

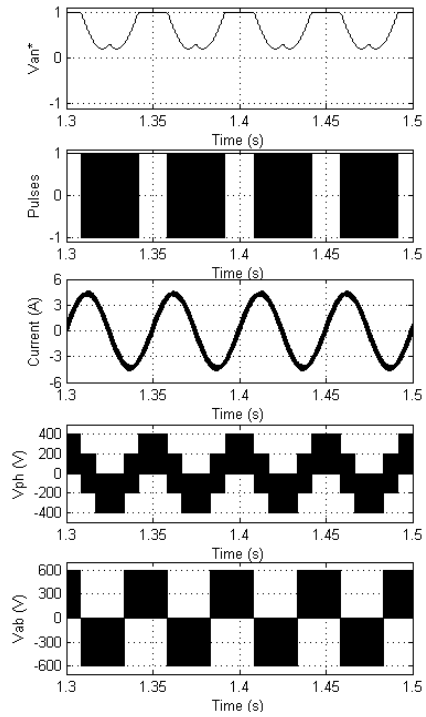

Figure 9 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for DPWMMAX algorithm at f=20 Hz and M=0.36

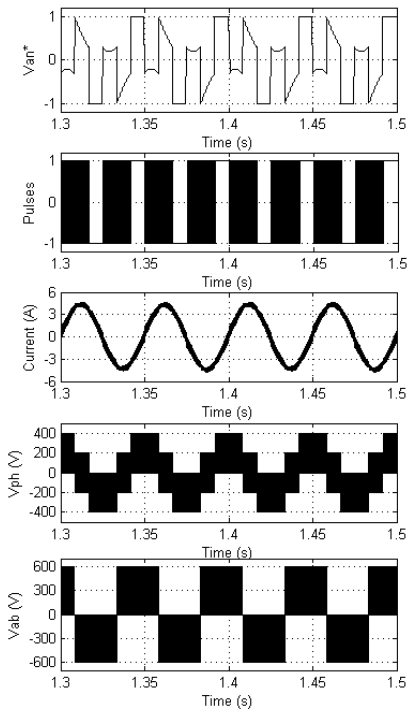

Figure 10 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for DPWMM0 algorithm at f=20 Hz and M=0.36

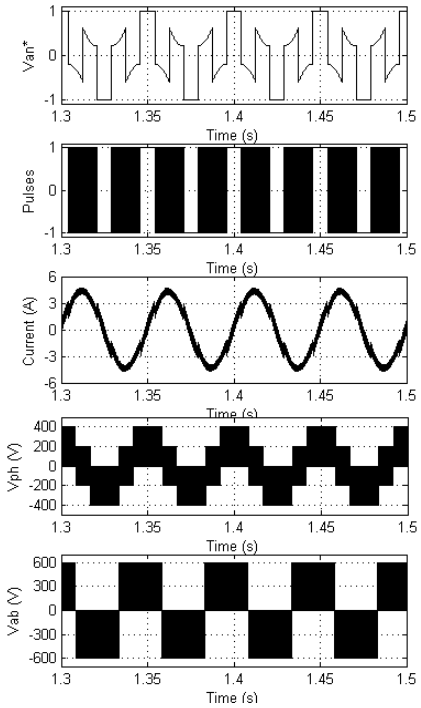

Figure 11 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for DPWMM1 algorithm at f=20 Hz and M=0.36

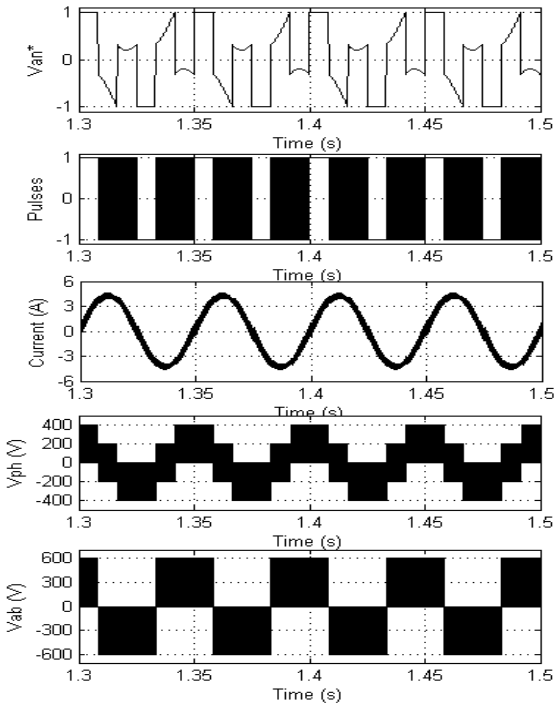

Figure 12 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for DPWM2 algorithm at f=20 Hz and M=0.36

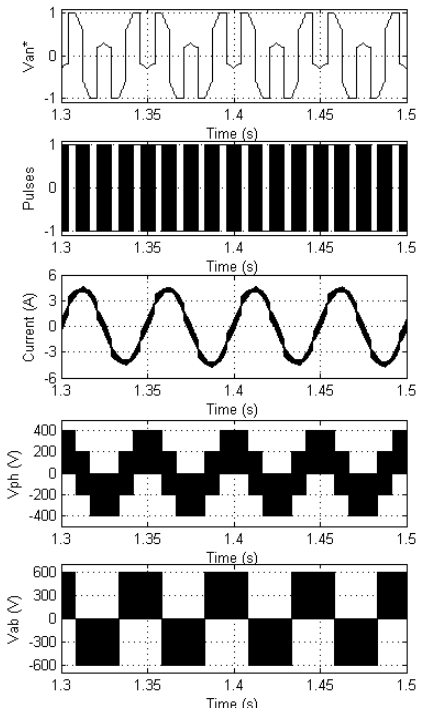

Figure 13 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for DPWM3 algorithm at f=20 Hz and M=0.36

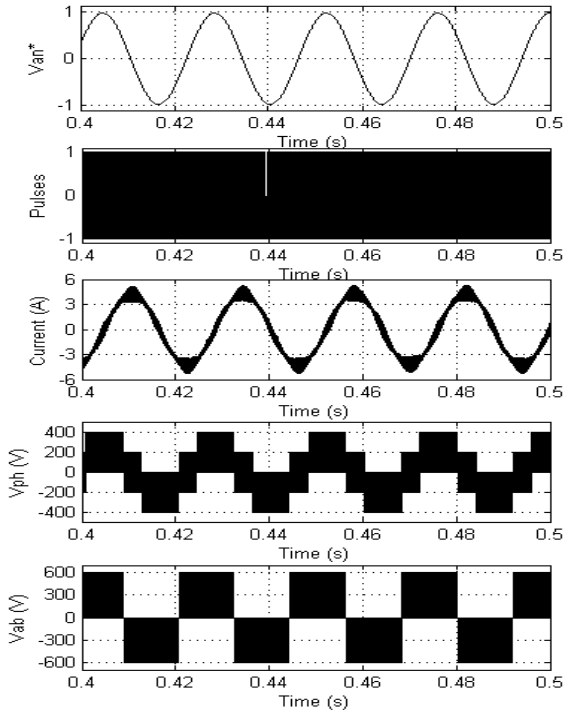

Figure 14 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for SPWM algorithm at f=42 Hz and M=0.76

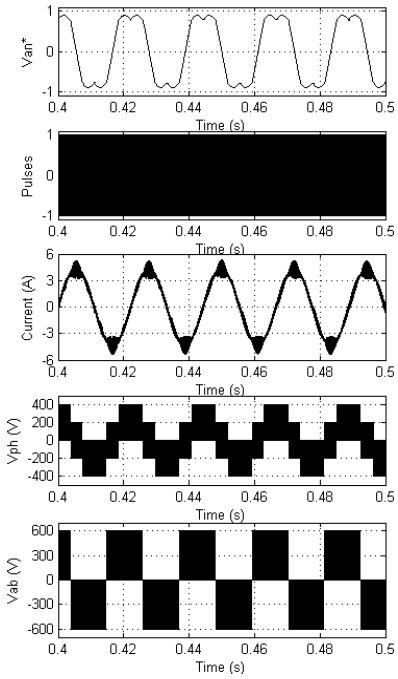

Figure 15 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for SVPWM algorithm at f=45 Hz and M=0.815

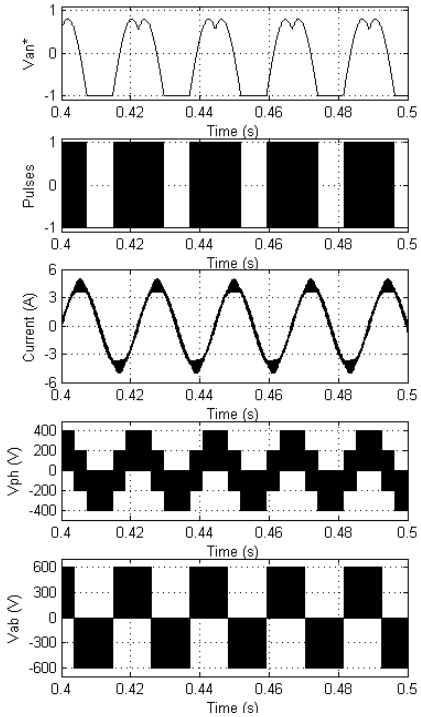

Figure 16 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for DPWMMIN algorithm at f=45 Hz and M=0.815

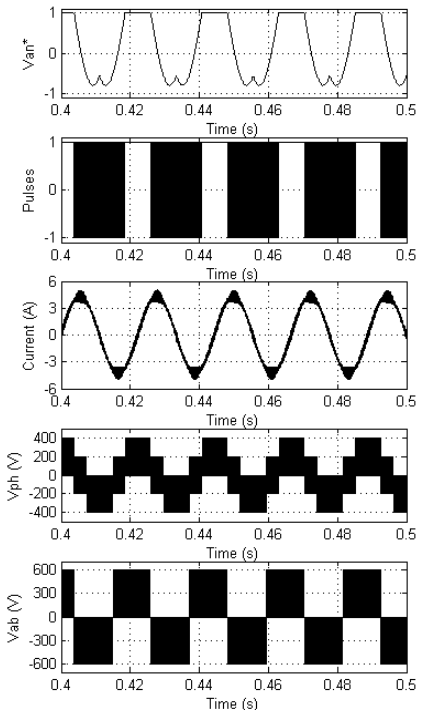

Figure 17 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for DPWMMAX algorithm at f=45 Hz and M=0.815

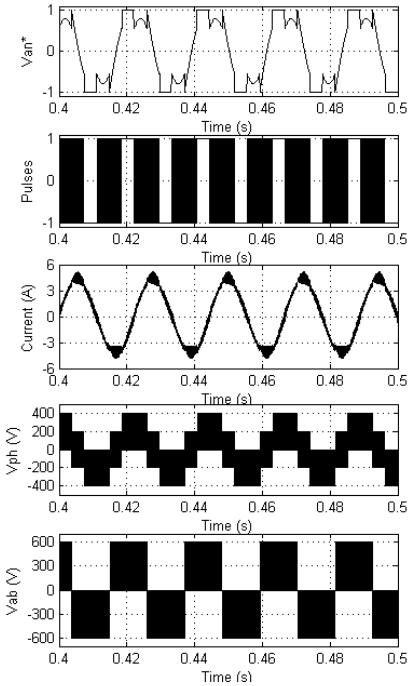

Figure 18 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for DPWM0 algorithm at f=45 Hz and M=0.815

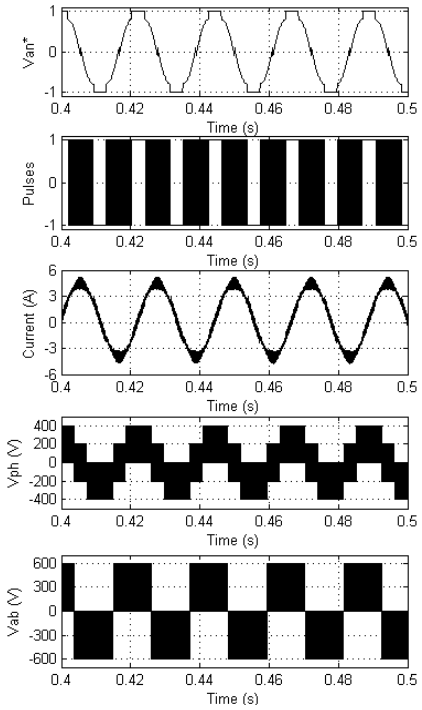

Figure 19 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for DPWM1 algorithm at f=45 Hz and M=0.815

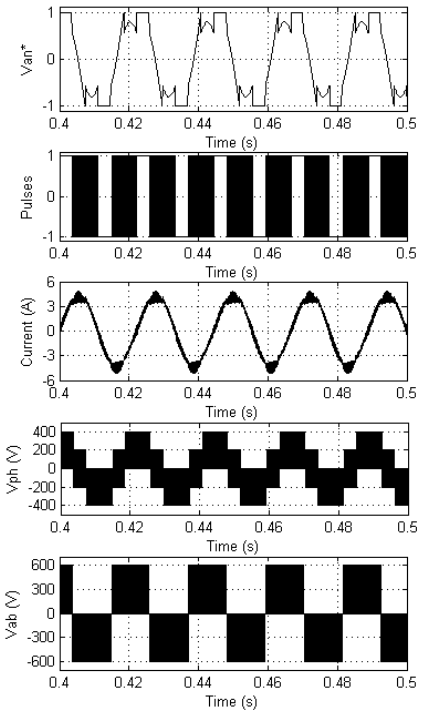

Figure 20 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for DPWM2 algorithm at f=45 Hz and M=0.815

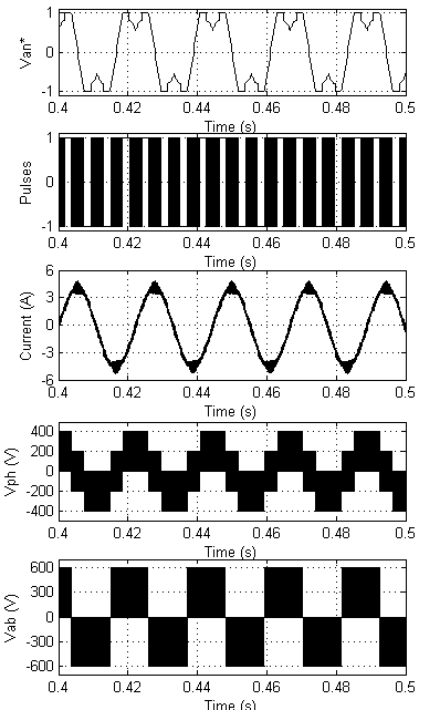

Figure 21 : Modulation wave, pulse pattern, steady state stator current, phase voltage and line voltage for DPWM3 algorithm at f=45 Hz and M=0.815

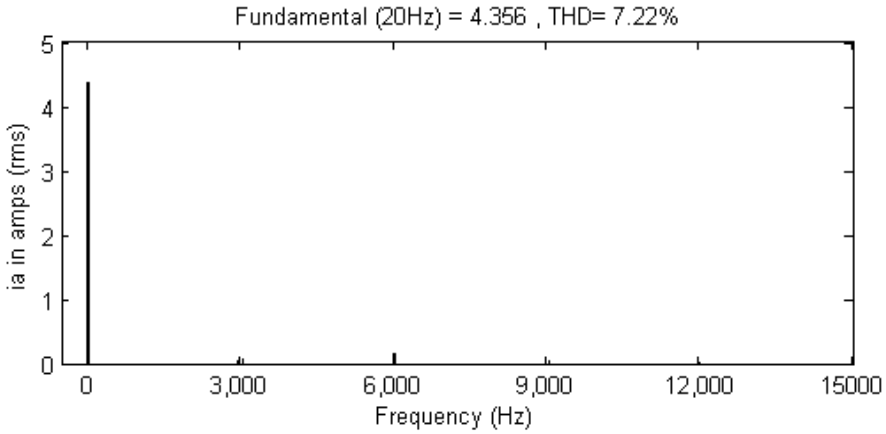

Figure 22 : Harmonic spectra of stator current for SPWM algorithm at f=20 Hz and M=0.36

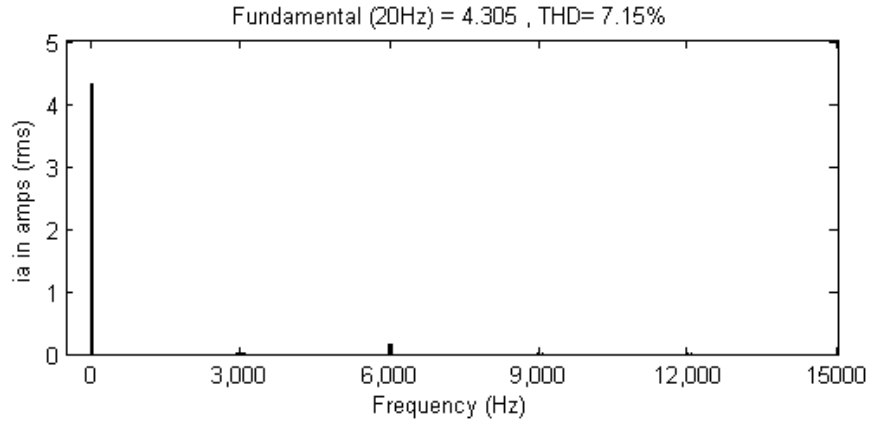

Figure 23 : Harmonic spectra of stator current for SVPWM algorithm at f=20 Hz and M=0.36

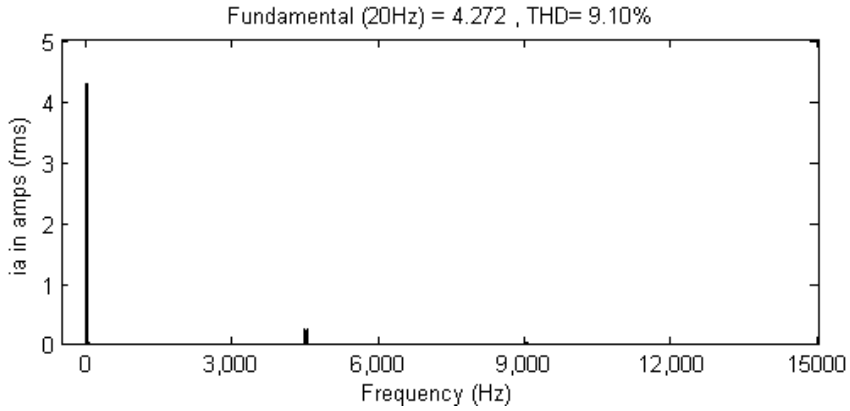

Figure 24 : Harmonic spectra of stator current for DPWMMIN algorithm at f=20 Hz and M=0.36

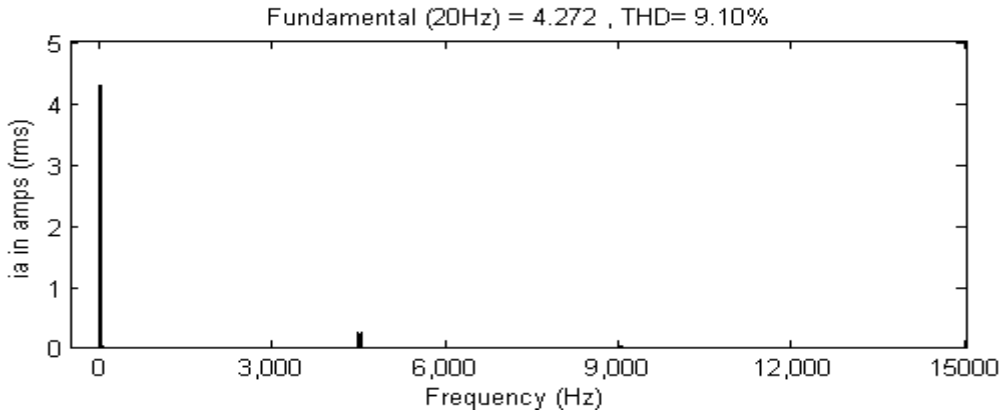

Figure 25 : Harmonic spectra of stator current for DPWMMAX algorithm at f=20 Hz and M=0.36

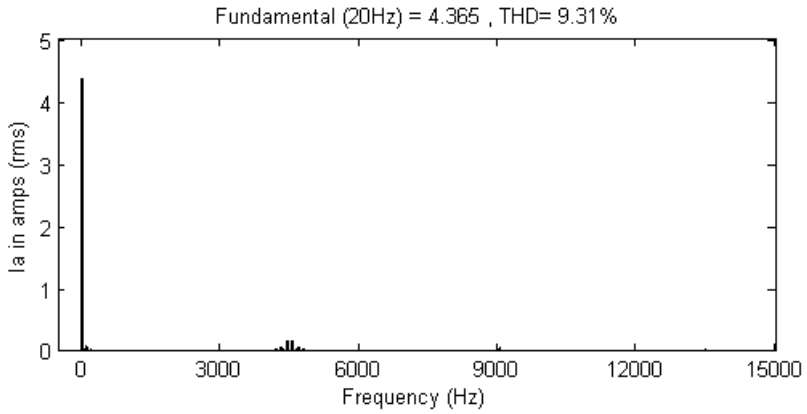

Figure 26 : Harmonic spectra of stator current for DPWM0 algorithm at f=20 Hz and M=0.36

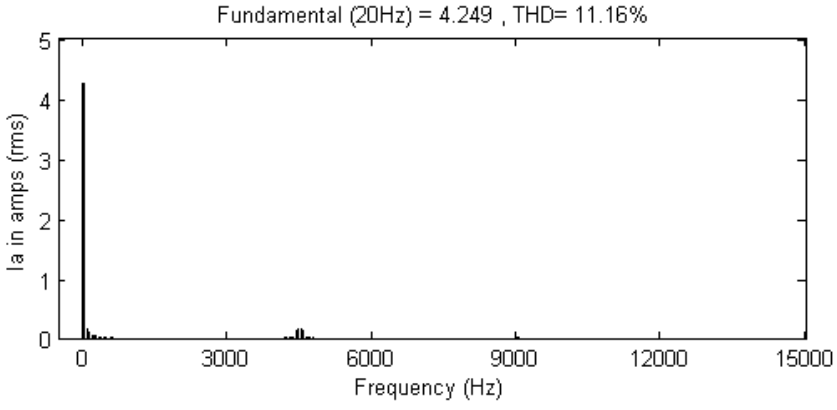

Figure 27 : Harmonic spectra of stator current for DPWM1 algorithm at f=20 Hz and M=0.36

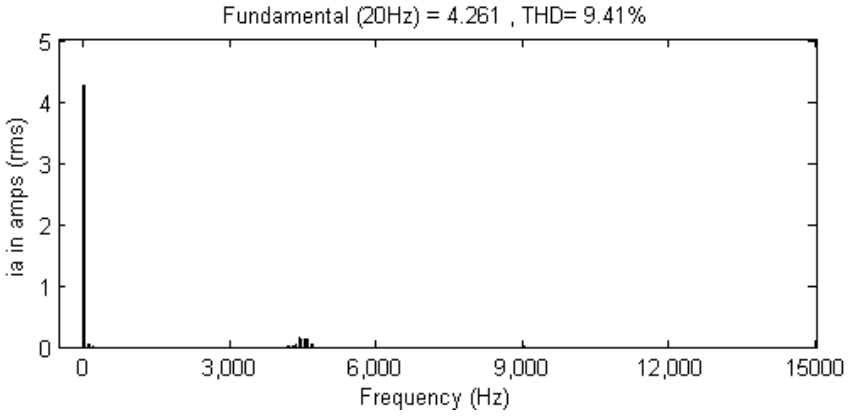

Figure 28 : Harmonic spectra of stator current for DPWM2 algorithm at f=20 Hz and M=0.36

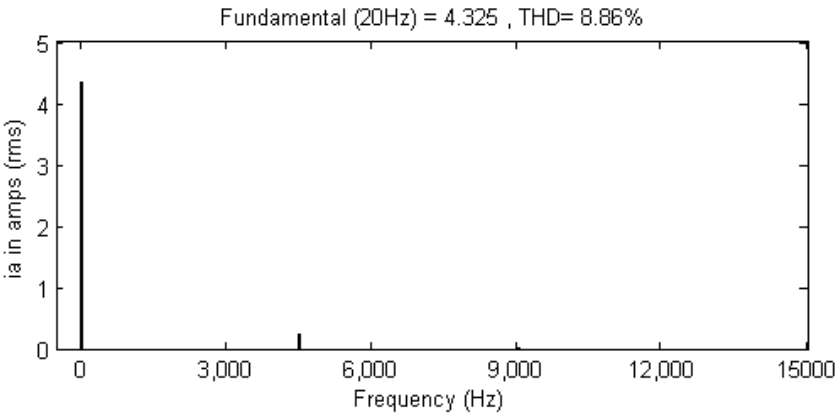

Figure 29 : Harmonic spectra of stator current for DPWM3 algorithm at f=20 Hz and M=0.36

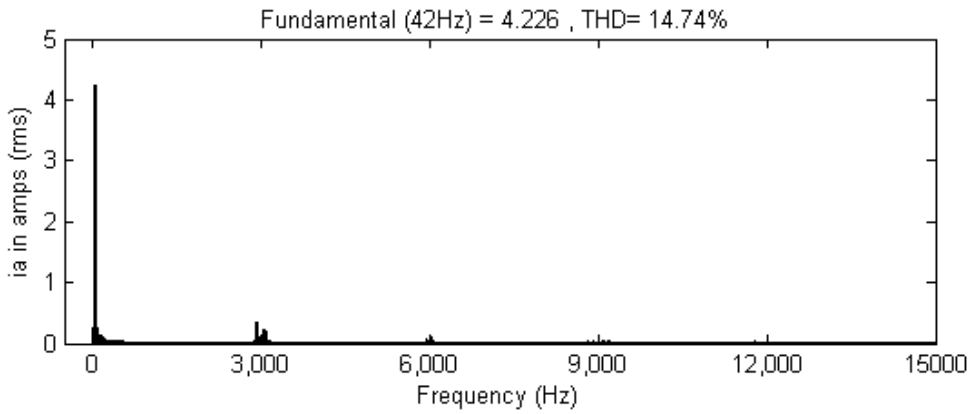

Figure 30 : Harmonic spectra of stator current for SPWM algorithm at f=42 Hz and M=0.76

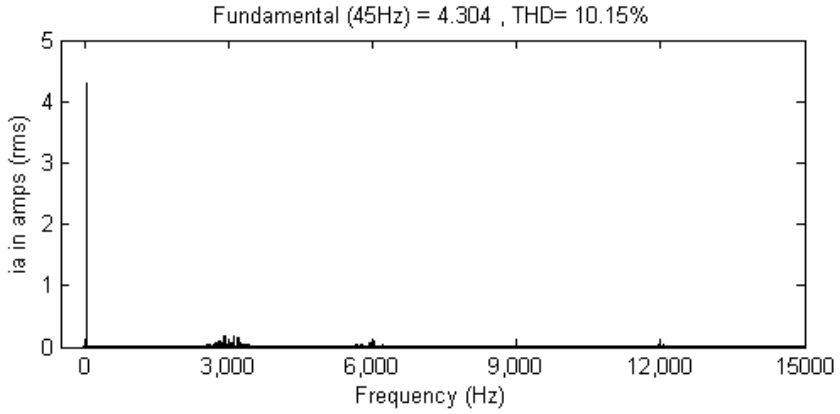

Figure 31 : Harmonic spectra of stator current for SVPWM algorithm at f=45 Hz and M=0.815

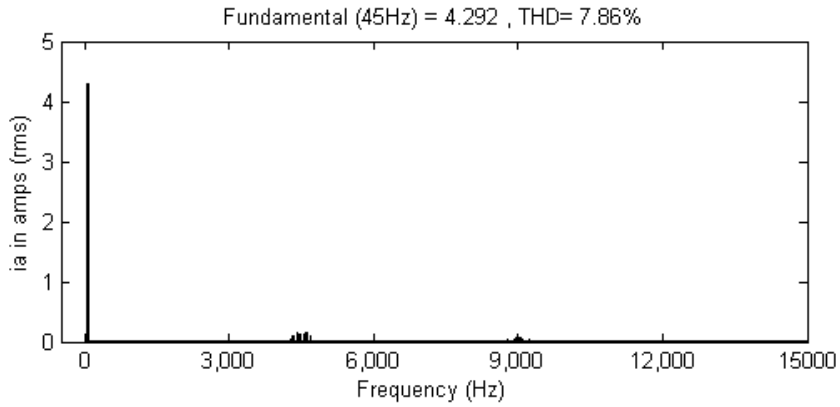

Figure 32 : Harmonic spectra of stator current for DPWMMIN algorithm at f=45 Hz and M=0.815

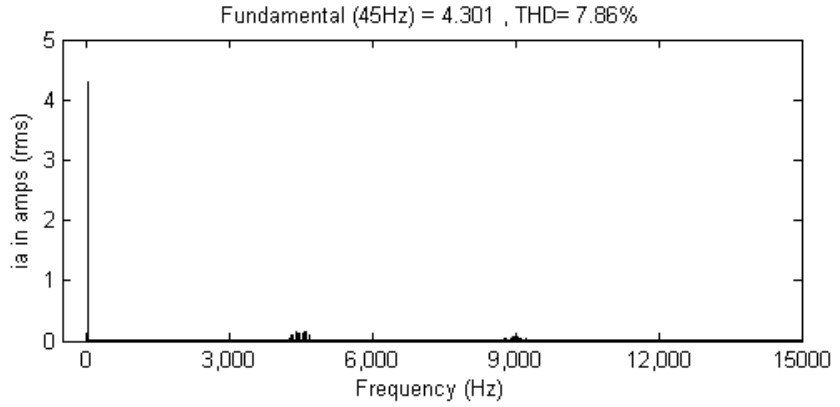

Figure 33 : Harmonic spectra of stator current for DPWMMAX algorithm at f=45 Hz and M=0.815

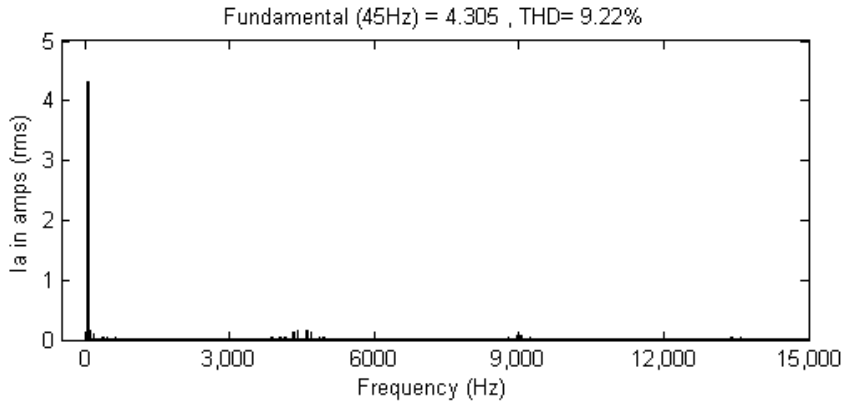

Figure 34 : Harmonic spectra of stator current for DPWM0 algorithm at f=45 Hz and M=0.815

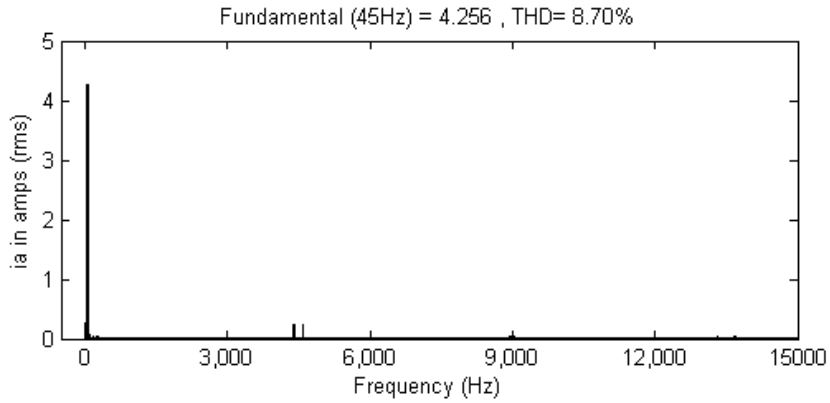

Figure 35 : Harmonic spectra of stator current for DPWM1 algorithm at f=45 Hz and M=0.815

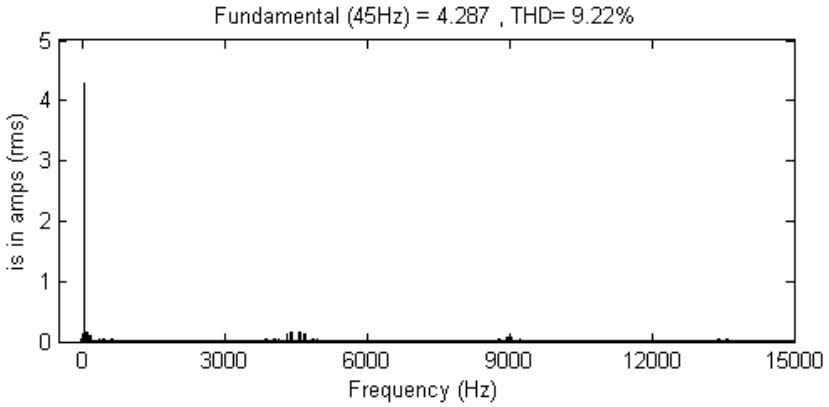

Figure 36 : Harmonic spectra of stator current for DPWM2 algorithm at f=45 Hz and M=0.815

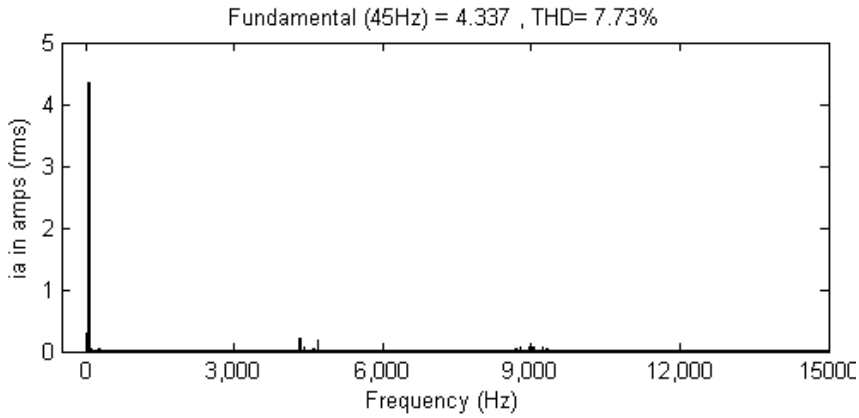

Figure 37 : Harmonic spectra of stator current for DPWM3 algorithm at f=45 Hz and M=0.815

Conclusions

A simple and novel space vector based UPWM algorithm has been developed and simulation results are presented in this paper. The proposed algorithm uses a generalized expression for offset time and by varying which various PWM algorithms are generated. Moreover, the proposed algorithm uses only reference phase voltages and eliminates the angle and sector calculations. By varying offset time different DPWM algorithms along with SVPWM are generated. In DPWM algorithms, the modulating signal ceases the pulses by 120 degrees in every fundamental cycle. From the simulation results, it can be observed that at lower modulation indices CPWM algorithms give good performance and at higher modulation indices DPWM algorithms give superior performance. But, at all modulation indices DPWM algorithms give less switching losses. Moreover, DPWM3 gives less harmonic distortion when compared to remaining DPWM algorithms.

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