

## Study and Simulation of SOI n-MOSFET Transistor Single Gate using SILVACO Software

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### Abstract

MOS Technology on massive substrate played a critical task during micro-electronic evolution. The regular reduction of transistors sizes leads today to nanometric devices. With this reduction, some parasitic physical effects, previously with no importance, became mostly amplified, leading to the end of MOSFETs technology on massive substrate. SOI technology gives a good alternative to that miniaturization. SOI technology allows the reduction of short channel effects that appear in nanometer devices (under 50nm node) and also allows micro-electronic evolution to continue. In this paper, we present simulation results we obtained using SILVACO TCAD tools relating to SOI n-MOSFET structures we have consider. We will also exhibit some simulation results we obtained relating to the influence of some parameters variation on our structure, that having a direct impact on their drain current.

**Keywords:** Silicon On Insulator"SOI"; FDSOI; PDSOI; SCE; SILVACO; Device Simulation.

### Introduction

Since the invention of the first transistor in 1947 [1], then the integrated circuit in 1958 [2] by Jack Kilby, microelectronics progresses has been considerable, both in terms of improved performance and increased complexity of circuits that of lower production costs. MOSFET transistors on silicon used in CMOS architecture are the main craftsmen's of this continual progression and overwhelmingly dominate semiconductors market. The improved of these transistors performance always requires more imagination on the part of component designers in order to respect the

new requirements of electronics industry for faster, smaller, low power and reliable ICs. However, with this frenetic race towards miniaturization, device feature sizes progress into deep-sub-micrometer regime under 50nm node for realizing better device performance and higher integration densities.

Accordingly, MOSFETs characteristics degrade, and some effects known as short channel effects appear, worsening the correct operation of CMOS devices. The importance of these effects and the complexity of the methods used to counter them led to the development of alternative transistor structures (new architectures) and new materials. These new architectures can be the possible alternatives to the bulk traditional MOSFETs. Thus, to achieve this goal laid down by the “International Technology Roadmap of Semiconductor” [3], new architectures using SOI MOSFETs had been very seriously considered to replace bulk MOSFET architecture.

Nowadays, SOI technology is considered to take the CMOS processing to its ultimate scalability in order to highlight the qualities and also the defects of SOI technology, we propose in this work to present, simulation results we obtained using SILVACO software for an SOI n-channel MOSFET with static biased.

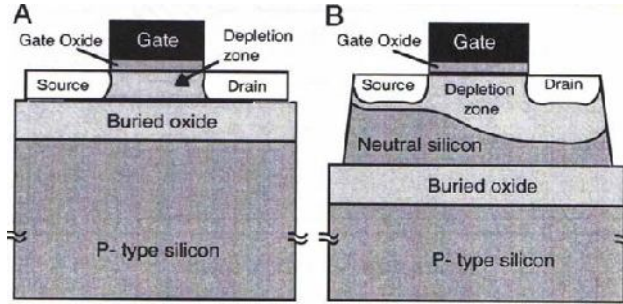
### **SOI Technology**

SOI technologies can be in general divided into two groups. In the first, a thin insulating layer is used to separate the active semiconductor layer from the semiconductor substrate.

These include Separation by IMplantation of OXYgen (SIMOX) [4], Zone Melting Recrystallization (ZMR) [5], Full Isolation by Porous Oxidized Silicon (FIPOS) [6], and Wafer Bonding (WB) [7]. In the second group, the semiconductor film is deposited directly onto an insulating substrate. This is the case for Silicon On Sapphire (SOS) [8], and Silicon On Zirconia (SOZ) [9].

In SOI technology, transistors are then built on a thin silicon layer. In fact, on the top on insulator layer, a thin film of silicon layer is used to build active devices and circuits. If this silicon film is thin enough the depletion zone below the gate extends all the way through the buried oxide, and the device is said to be fully depleted (Figure A.), if not it is called partially depleted (Figure B). The significant feature of fully depleted SOI MOSFET is that the current drive is higher than in bulk MOSFET and its subthreshold slope is sharper due to an much smaller body factor [10].

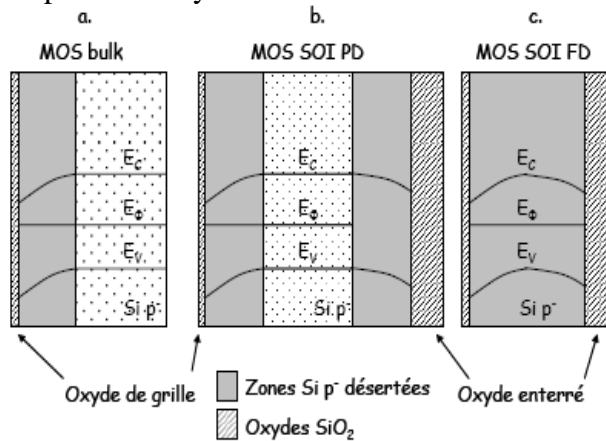
Generally, SOI MOSFETs that have a thin SOI layer (normally <50 nm) and have all body areas under the channel depleted, are called complete or fully depleted SOI MOSFET, where the buried oxide reduce dramatically the junction capacitance [11]. Conversely, elements that have a thick SOI layer (normally >100 nm) and have some areas at the bottom of the body area that are not depleted, are called partially depleted SOI MOSFET.



**Figure 1:** (A) Fully depleted SOI MOSFET, (B) -Partially depleted SOI MOSFET [12].

**Determination of Depletion Zone Thickness  $X_{dmax}$**

Silicon active layer thickness called  $T_{si}$  is one of the key parameters in the classification and operation of SOI MOSFETs. According to this thickness localized between gate oxide and buried oxide, transistor operation and various physical phenomena in the components vary.



**Figure 2:** Energy band diagram of MOS structures [13].

The interface zones between oxide and silicon are deserted from the majority carriers (p+) and a depletion zone exists, in a thick-film SOI device, the silicon film thickness is larger than twice the maximum depletion width [14]:

$$X_{dmax} = \sqrt{\frac{4\epsilon_{Si}\Phi_F}{qN_A}} \quad \Phi_F = \frac{KT}{q} \ln\left(\frac{N_A}{n_i}\right)$$

Where

$\Phi_F$  being the fermi potential is given by:

$$\Phi_F = \frac{KT}{q} \ln\left(\frac{N_A}{n_i}\right)$$

$\epsilon_{Si}$  : Silicon dielectric constant,  $\epsilon_{Si} = 11,8.\epsilon_0$ ,

$\epsilon_0$ : vacuum diélectric constant , $\epsilon_0 = 8,85.10^{-12}$  F/m

$q$  : electron charge,  $q = 1,602.10^{-19}$  C,

$N_A$  : Silicon layer doped concentration, in our structure SOI n-MOSFET,

$N_A=1 \times 10^{17}$  atomes/  $\text{cm}^3$ ,

$n_i$  : intrinsic carrier concentration,

$n_i=1.4 \times 10^{10}$  atomes/ $\text{cm}^3$ ,

$K$  : Boltzmann Constant,  $K = 8,617385.10^{-5}$  eV/K,

$T$ : temperature ,  $T=300^\circ\text{K}$ ,

$$\frac{KT}{q} = 0.026\text{V}$$

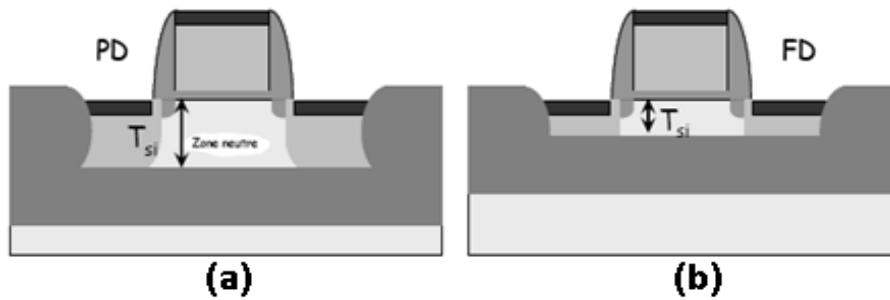
$$\Phi_F = \frac{KT}{q} \ln\left(\frac{N_A}{n_i}\right) = 0.41\text{V}$$

$$X_{d\max} = \sqrt{\frac{4\epsilon_{\text{si}}\Phi_F}{qN_A}} = 1.03 \times 10^{-5}\text{cm}$$

$$X_{d\max} \approx 0.1\mu\text{m}$$

**Table1:** SOI MOSFETs Function according to depletion zones thickness

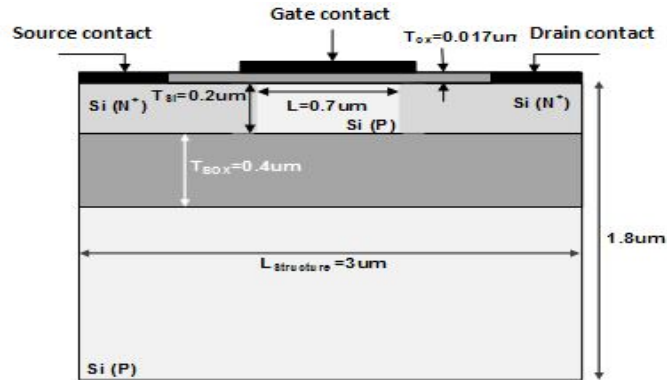
	$T_{\text{si}} < X_{d\max}$	$X_{d\max} < T_{\text{si}} < 2X_{d\max}$	$T_{\text{si}} > 2X_{d\max}$
Silicon film	Fully-Depleted mode	Not Fully-Depleted Depend on bias conditions	Partially-Depleted mode.



**Figure 3:** (a) Structure of partially depleted SOI MOSFET, (b) Structure of fully depleted SOI MOSFET [13].

### Device Simulation

Numerical simulation is an extremely helpful tool for detailed investigation of physical phenomena, which determine electrical characteristics of semiconductor devices. Simulation results we present in this study had been obtained using Atlas Silvaco Software [15].



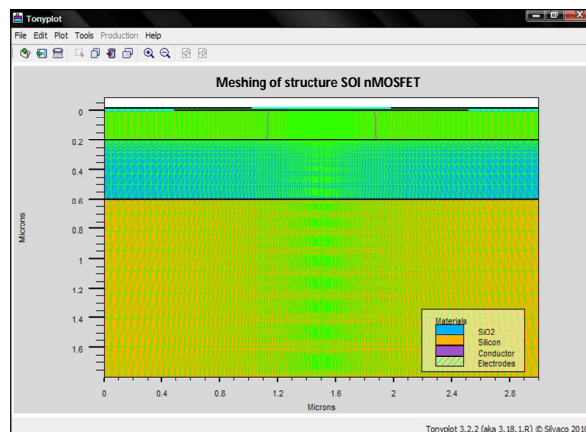
**Figure 4:** Basic structure of the SOI n-MOSFET.

The starting point for our simulations is a basic structure represented in Figure 4. The different parameters of our structure are assumed as follows:

**Table 2:** Parameters of the SOI n-MOSFET transistor.

Drain length and Source length	1μm
Gate length	1μm
Channel length	0.7μm
Gate oxide thickness $T_{OX}$	0.017μm
Silicon film thickness $T_{si}$	0.2μm
Buried oxide thickness $T_{BOX}$	0.4μm
substrate Thickness	1.2μm
Depth junction	0.52μm
Substrate concentration	$1 \times 10^{17} \text{ cm}^{-3}$
Drain and Source concentration	$1 \times 10^{20} \text{ cm}^{-3}$

The below structure is obtained using ATLAS device simulation using. The thickness of the silicon film is 0.2 μm. This ensures that the channel is partially depleted.



**Figure 5:** Mesh Structure of device Simulation SOI n-MOSFET transistor.

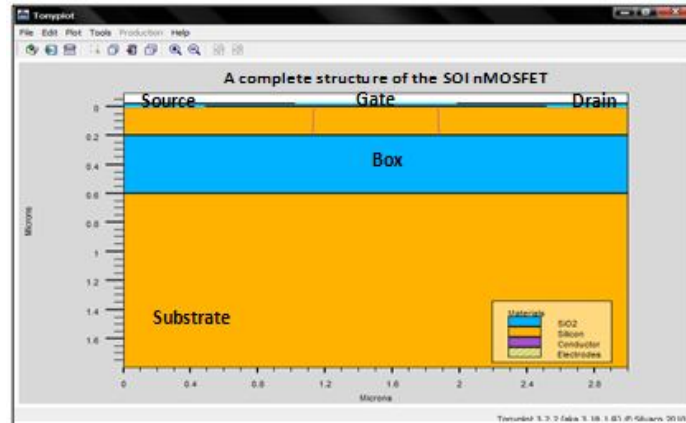


Figure 6: Final device Structure of SOI n-MOSFET transistor.

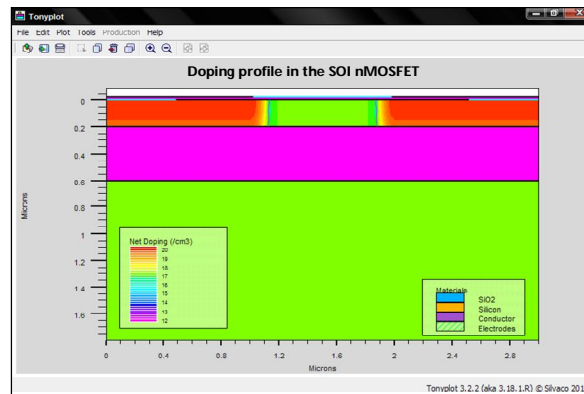


Figure 7: The doping profile of SOI n-MOSFET transistor.

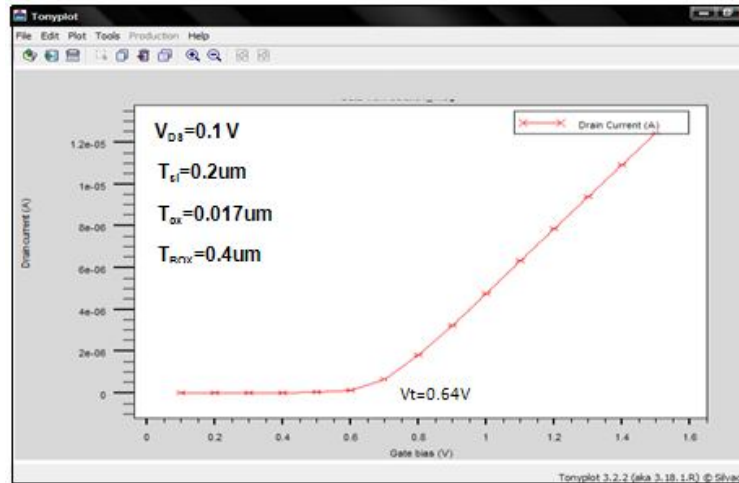
### Simulation Results and Discussion

Figure 8 illustrate  $I_{DS}-V_{GS}$  characteristic of the transistor SOI n-MOSFET which we obtained during our simulations with a biasing  $V_{DS}$  of about 0.1 V.

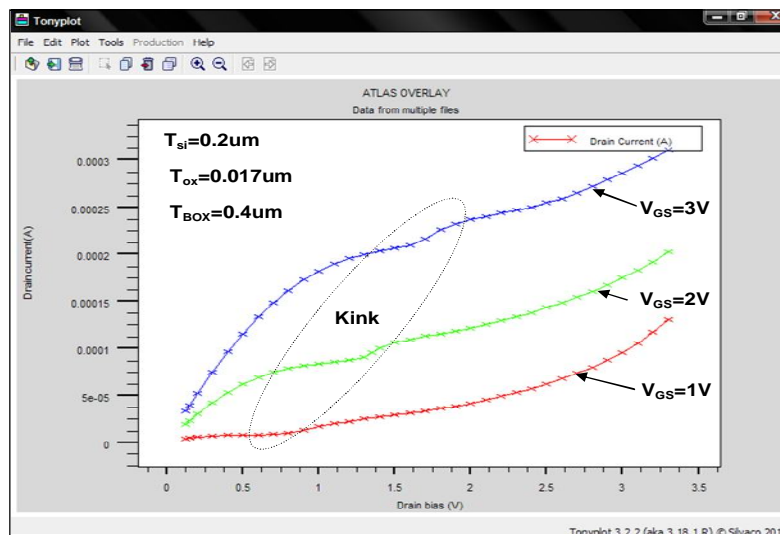
We let us can notice that our transistor is busy starting from a threshold tension of about 0.64V.

Figure 9 illustrate  $I_{DS} -V_{DS}$  characteristic with  $V_{GS}$  constant.  $I_{DS} - V_{DS}$  characteristics with  $V_{GS}$  constant makes it possible to highlight two adverse effects for such structure to know: the Kink effect and the parasitic bipolar transistor effect.

The Kink effect appears beyond a certain value of the drain bias and results from the high electric field in this area and from the mechanism of ionization by impact. We can be also observed the parasitic bipolar transistor.



**Figure 8:** Simulated  $I_{DS}$ – $V_{GS}$  characteristics of SOI n-MOSFET transistor.



**Figure 9:** Simulated  $I_{DS}$ – $V_{DS}$  characteristics of SOI n-MOSFET transistor.

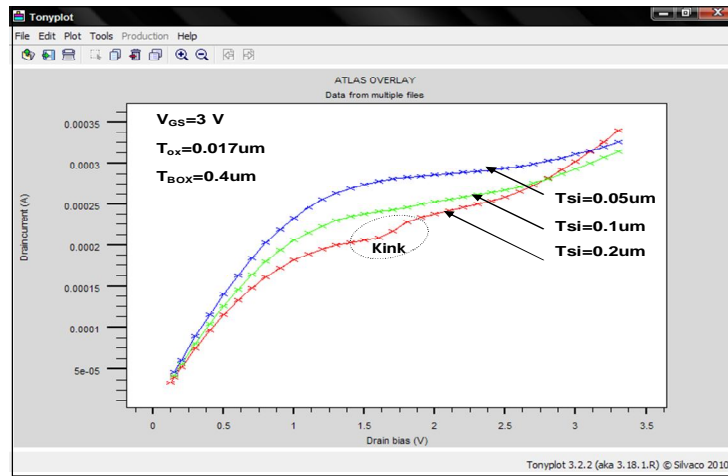
### **Influence of Parameters Variation on the Drain Current**

In order to study the influence of our structure parameters such as silicon body thickness oxide on its electrical characteristics, some parameters are modified. We examine then the effect of their variation on the considered structure drain current.

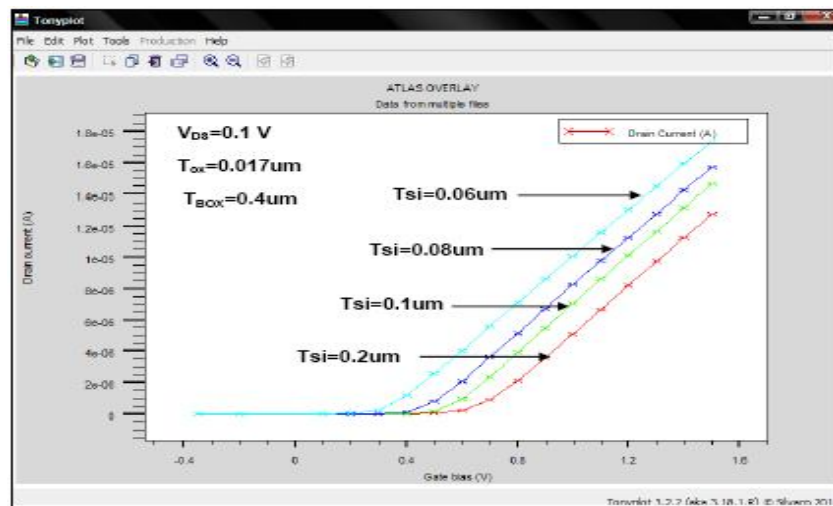
#### **Influence of silicon body thickness variation on $I_{DS}$ current**

Scaling silicon film thickness is desirable for better short channel behavior and reduced floating body effect. Consequently it is practical to consider the impact of silicon body thickness on the device performance.

Figures 10 and 11 show the output and the transfer characteristics for different silicon film thickness  $T_{si}$ .



**Figure 10:**  $I_{DS}$ - $V_{DS}$  characteristics of PDSOI n-MOSFET transistor for  $T_{si}=0.2$ , 0.1 and 0.05  $\mu\text{m}$ .



**Figure 11:**  $I_{DS}$ - $V_{GS}$  characteristics of SOI n-MOSFET transistor for  $T_{si}=0.2$ , 0.1, 0.08 and 0.06  $\mu\text{m}$ .

Our simulation results allow observing that for a significant  $T_{si}$ , ( $T_{si} > 0.2 \mu\text{m}$ ), the depletion zone under the conducting channel does not extend sufficiently in-depth to reach buried oxide, we obtain then a Partially Depleted SOI MOSFET called “PDSOI MOSFET”. This effect appears in  $I_{DS}$ - $V_{DS}$  characteristics by the emergence of a “kink”.

The kink appears essentially for n-channel PD SOI n-MOSFETs above a certain value of  $V_{DS}$  voltage. At room temperature, Kink effect is not observed in bulk devices when substrate or well connections are provided, however kink effect can be observed in bulk MOSFET’s operating at low temperatures.



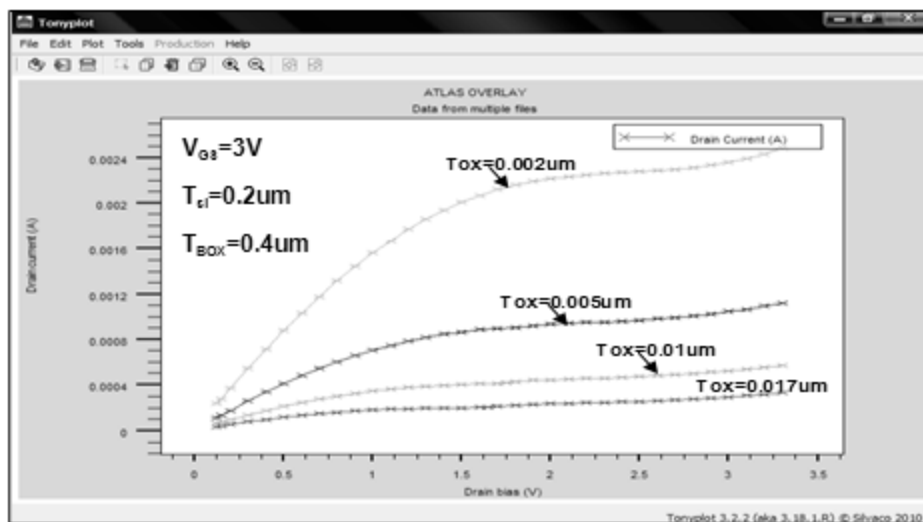
Kink effect is one of the principal effects of the floating substrate, started by the accumulation of carriers produced by impact ionization in the silicon film. This effect is translated in PDSOI transistors by the increase of drain current and an electric noise in its saturation region. When we reduce silicon film thickness, this depletion layer reach the BOX, we obtain a Fully Depleted SOI MOSFET “FDSOI”. We can observe that the kink effect does not appear for FDSOI MOSFET on  $I_{DS}$ - $V_{DS}$  characteristics. It is also important to notice that a thin silicon film allows a better electrostatic control of the gate on the channel leading to threshold voltage reduction.

In fact threshold voltage increases with the increase in the thickness of the silicon film, but after a certain limit of  $T_{si}$ , when its thickness is greater than  $0.2 \mu\text{m}$  we obtain a PD SOI structure, where threshold voltage remains the same and is insensitive to the thin-film thickness since the depletion region is independent of this film thickness.

Conversely, due to the neutral region in the thick film of the PDSOI n-MOSFET, parasitic bipolar device structure leading to floating body effect is more serious. Furthermore, in partially-depleted silicon thin-film SOI CMOS devices, due to the neutral region, an unsmooth transition in the drain current characteristics-kink effect is identified.

### Influence of $T_{ox}$ variation on $I_{DS}$ current

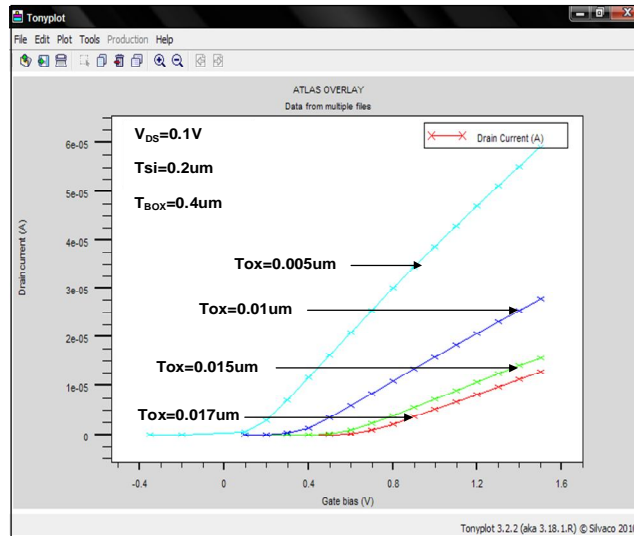
Scaling oxide thickness is desirable for better drain current. Consequently it is practical to consider the impact of  $T_{ox}$  thickness on the device performance. Figures. 12 and 13 exhibit the output and the transfer characteristics at different gate lengths.



**Figure 12:**  $I_{DS}$ - $V_{DS}$  characteristics of PDSOI n-MOSFET transistor for  $T_{ox}=0.017, 0.01, 0.005$  and  $0.002 \mu\text{m}$ .

Figure 12 illustrates  $I_{DS}$ -  $V_{DS}$  characteristics for PD SOI n-MOSFET transistor ( $T_{si}=0.2\mu m$ ) at different oxide thickness.

At shorter oxide thickness, the drain saturation current increases strongly. We can conclude for this variation that thinner gate oxides lead to product higher drain currents and transconductances, and a better pinch-off behavior. Consequently it is recommended to choose the lowest possible oxide thickness.



**Figure 13:**  $I_{DS}$ - $V_{GS}$  characteristics of SOI n-MOSFET transistor for  $Tox=0.017$ ,  $0.015$ ,  $0.01$  and  $0.005\mu m$ .

Figure 13 illustrate transfer characteristics for a PD SOI n-MOSFET transistor ( $T_{si}=0.2\mu m$ ) at different oxide thickness. We can observe that threshold voltage decrease for lower oxide thickness. Indeed, oxide thickness decreasing leads to  $C_{ox}$  increasing and consequently to threshold voltage decreasing.

We can then conclude that gate oxide thickness has a very big effect on the threshold voltage.

### **Influence of gate length variation on $I_{DS}$ current**

This section deals with the study of gate length variation effect on the electrical device characteristics. In order to achieve this task, the channel length transistor was held constant; however the gate length covers part or the entire channel. The influence of gate length variation effects on drain current was studied by holding the channel length constant and equal to  $0.7\mu m$ .

Figures 14 and 15 illustrate the output and the transfer characteristics at different gate lengths for a FD SOI n-MOSFET. Figures 16 and 17 illustrate the output and the transfer characteristics at different gate lengths for a PD SOI n-MOSFET.

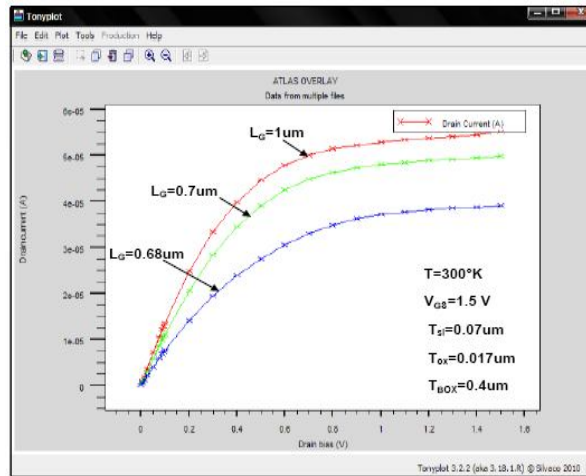


Figure 14: Output characteristics for a FDSOI n-MOSFET at different gate lengths.

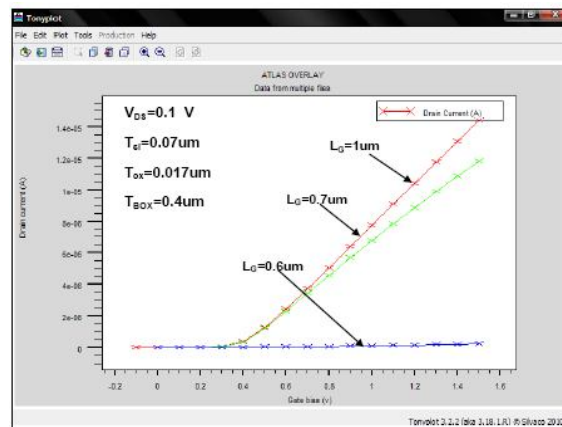


Figure 15: Transfer characteristics for a FDSOI n-MOSFET at different gate lengths.

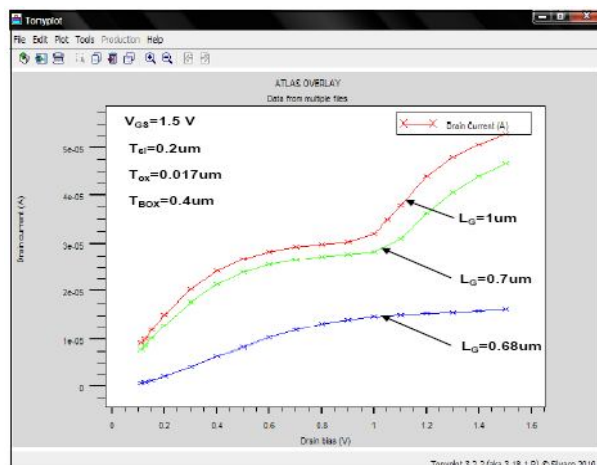
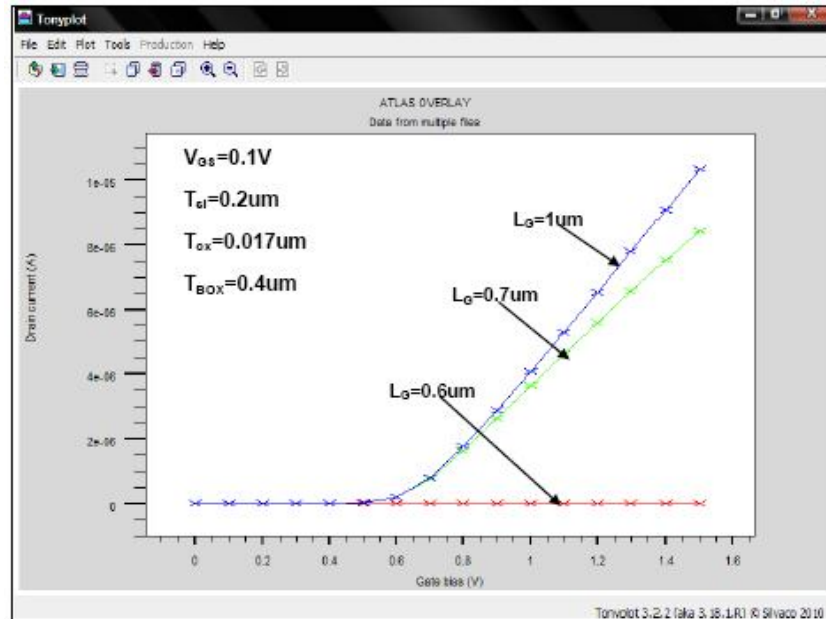


Figure 16: Output characteristics for a PDSOI n-MOSFET at different gate lengths.



**Figure 17:** Transfer characteristics for a PDSOI n-MOSFET at different gate lengths.

When the gate length increases, the drain current characteristics slope increase to, and therefore the transistor transconductance increases. At shorter gate lengths a threshold voltage roll off can be observed. In fact we can conclude that gate length must be chosen judiciously because the gate loss its control on the channel when  $L_{gate}$  is less significant than  $L_{channel}$ .

## Conclusion

From these simulations results of the structure of the SOI n-MOSFET transistor and the Influence of parameters variation on the drain current obtained using SILVACO software, we noted the following comments:

Silicon body thickness  $T_{si}$  is a parameter can not be ignored and have an impact on the operation of MOS transistors on SOI substrate, it is according to the thickness between the gate oxide and buried oxide, the work and the various physical phenomena in the components vary.

Oxide thickness  $T_{ox}$  is an important technological parameter characterizing the SOI MOSFET transistors, and we must decide wisely. For the reduction of the thickness  $T_{ox}$  improves the performance of these transistors in terms of current which increases as drain  $T_{ox}$  decreases.

The change in  $L_G$  geometrical parameter representing the gate length is best for the structure designed. The parameter may be changed during the reduction or increase in gate length is the value of the drain current. The reduction in the gate length can not do so is limited by the value of the effective channel length.

Indeed the value of  $L_G$  in our structure can not be less than  $0.7\mu m$  which is the effective length of the channel.

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